

hp kayak xu700

Technical Reference Manual



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Preface

This manual is a technical reference and BIOS document for engineers and technicians providing system level support. It is assumed that the reader possesses a detailed understanding of AT-compatible microprocessor functions and digital addressing techniques.

Technical information that is readily available from other sources, such as manufacturers' proprietary publications, has not been reproduced.

This manual contains summary information only. For additional reference material, refer to the bibliography on the following page.

For all warning and safety instructions, refer to the user guide delivered with the PC Workstation.

Conventions

The following conventions are used throughout this manual to identify specific numeric elements:

Hexadecimal numbers are identified by a lower case h. For example, 0FFFFFFFh or 32F5h

Binary numbers and bit patterns are identified by a lower case b. For example, 1101b or 10011011b

Bibliography

Documentation can be downloaded from the HP web site:

www.hp.com/go/kayaksupport.

HP Kayak XU700 User's Guide

Available in English, French, Italian, German, Spanish and Swedish.

HP Kayak XU700 Troubleshooting Guide

Available in English, French, Italian, German, Spanish and Swedish.

 $\hfill\Box$ HP Kayak XU700 PC Workstation Service Handbook Chapter — Available in English only.

Extra Information Can Be Obtained At:

Extra Information Can Be \square nVIDIA graphics cards

http://www.nvidia.com

☐ ELSA graphics cards

http://www.elsa.com

☐ Matrox graphics cards

http://www.matrox.com

☐ Intel Chipsets. Intel I850 chipset http://developer.intel.com

☐ Intel Pentium 4 Processor

http://developer.intel.com

This manual describes the *HP Kayak XU700 Minitower PC Workstation* and provides detailed system specifications.

This chapter introduces the external features, and lists the specifications and characteristic data of the system. It also provides a summary of the documentation available.

HP Kayak XU700 PC Workstation Overview

The *HP Kayak XU700 PC Workstation* is based on the ATX form factor. The following table provides an overview of the system.

Feature	Description		
System Board	Dimensions of 12-inches x 9.6-inches in an Extended-ATX (E-ATX) package		
Processor	Intel Pentium ® 4 processor. Socket 423 Processors from 1.4 GHz and upwards with a quad pumped 100 MHz FSB (Front Side Bus).		
Cache Memory (integrated in processor package)	Level-One: 16 KB code, 16 KB data.Level-Two: i256 KB.		
Internal Processor Clock Speed	1.4 GHz, 1.5 GHz and higher speeds with a quad pumped 100 MHz FSB.		
Chipset	Intel® Chipset (1850) including Memory Controller Hub (MCH) Host Bridge, Input/Output Controller Hub (ICH) for input/output sub-system.		
Super I/O Chip	NS 87364.		
BIOS (Basic Input/Output System)	Based on Phoenix core including: 4 M/bits of flash memory. Support for PCI 2.2 Specification. Support for RIMM memory modules.		
Firmware - BIOS	Flash EEPROM: Intel's Firmware hub concept.		

Feature	Description			
HP MaxiLife Utility	Hardware monitoring utility that monitors system components via the SMBus and a LCD status panel.			
Operating System	All models are preloaded with Windows 2000.			
Main Memory	2 pairs of RIMM sockets supporting 2 or 4 PC800 RDRAM memory modules. Each pair of memory sockets must contain identical memory modules (identical in size, speed and type). That is, sockets A1 and B1 must contain identical modules, and sockets A2 and B2 must contain identical modules (or continuity modules).			
	If only two RDRAM modules are installed, use the sockets marked A1 and B1. The other two sockets (A2 and B2) must contain continuity modules Models are supplied with non-ECC RDRAM modules. Both ECC and non-ECC modules are available. Up-to-date memory upgrades are listed on the HP PC Accessories website at: www.hp.com/go/pcaccessories			
Mass Storage	 Seven shelves supporting: Two front-access, third-height 3½-inch (one for the floppy disk drive and one free) (height 1"); Three front-access, half-height, 5¼-inch drives (height 1.0"); Possibility of installing two 3½-inch hard disk drive in one of the 5¼-inch shelves using an adapter tray (available as an accessory). Two internal 3½-inch hard disk drives (height 1.0"). 			
SCSI Controller	Adaptec Ultra 160 SCSI PCI card (optional).			
IDE Controller	All models include an integrated Ultra ATA-100 controller that supports up to four IDE devices.			
Graphics Controllers	 nVIDIA Quadro2 MXR with TwinView. Matrox Millennium G450-Dual monitor AGP graphics controller with 16 MB SGRAM graphics memory (maximum configuration). 			

Feature	Description			
Accessory Card Slots	One AGP Pro Universal 4X 32-bit slot supporting: ■ 1.5V AGP cards (≤25W) ■ 1.5V AGP Pro Cards (≤50W) High power > 50W AGP Pro and 3.3V AGP cards are not supported.			
	Five 32-bit 33 MHz PCI (Peripheral Component Interconnect) slots supporting all bridges and multi-function PCI devices. All five PCI slots comply with the PCI Specification 2.2. PCI slot 5 contains a LAN interface board, PCI slot 4 is for a SCSI interface board (some models only).			
LAN Card	All models are supplied with an HP 10/100BT PCI Ethernet Adapter LAN card installed in PCI slot 5, supporting Wake-On LAN (WOL) and PCI 2.2 Specification.			
CD-ROM Drive	Models include either an IDE 48X CD-ROM, CD-RW drive or DVD drive.			
Audio	Integrated on the system board CrystalClear™ CS4299 Audio Codec 97 version 2.1.			
System Board Connectors:	 One flexible disk drive connector Two ATA-100 IDE connectors (for up to four IDE devices) One CD-IN audio connector Internal speaker connector WOL connector Battery socket Status panel connector Main power supply connector and ATX 12V power connector Auxiliary power connector (used on MT models only) Main chassis fan connector Processor fan connector PCI card fan connector Chassis intrusion connector Thermal sensor connector 			

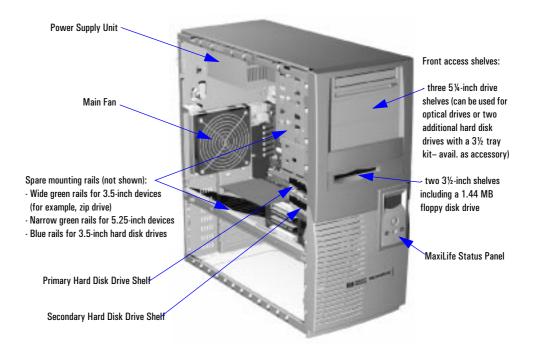
HP Kayak XU700 PC Workstation Overview

Feature	Description
Rear Connectors (color coded)	 Keyboard/Mouse HP enhanced keyboard with mini-DIN connector HP enhanced scrolling mouse with mini-DIN connector 25-pin parallel Mode: Centronics or bidirectional modes (ECP/EPP) Parallel port: 1 (378h, IRQ 7), 2 (278h, IRQ 5), or Off. 9-pin serial (two, buffered) Standard: Two UART 16550 buffered serial ports (both RS-232-C). Serial Ports A and B: 2F8h (IRQ 3), 2E8h (IRQ 3), 3F8h (IRQ 4), 3E8h (IRQ 4), or Off— (if one port uses 2xxh, the other port must use 3xxh). Dual USB connectors Audio LINE IN jack (3.5 mm) MIC IN jack (3.5 mm) MIC IN jack (3.5 mm)

Package for the Minitower Models

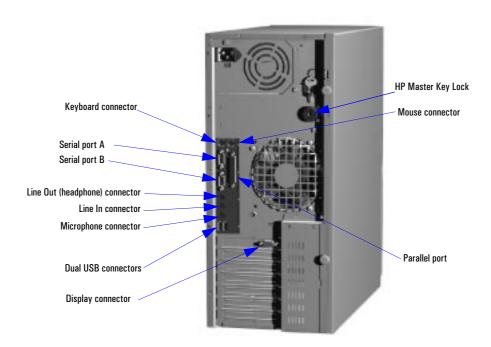
The following two diagrams show the front and rear views of the *HP Kayak XU700 Minitower PC Workstation*.

Front and Side Views



Internal Features

Rear View



Internal Features

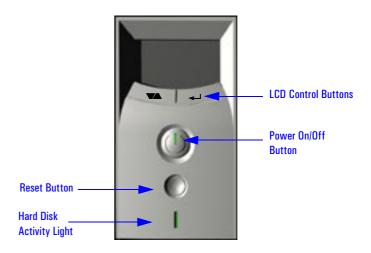
The core architecture of the *HP Kayak XU700 PC Workstation* is constructed around: Memory Controller Hub (MCH), Input/Output Controller Hub (ICH) and the Host bus.

The *HP Kayak XU700 PC Workstation* supports a Pentium IV processor. This processor is described on page 57.

The components of the system board are described in chapter 2; the graphics, network and SCSI devices are described in chapter 3; mass storage devices are described in chapter 4; the HP BIOS routines are summarized in chapter 5; and the Power-On Self-Test routines are described in chapter 6.

HP Kayak XU700 Minitower Front Panel

The front panel of *HP Kayak XU700 Minitower PC Workstation* has the following features:



- Liquid Crystal Display (LCD). LCD error messages and available menus are described on page 97.
- *On/Off LED*. There are five states:

Blank. Indicates that the computer is turned off.

Green. Indicates that the computer is turned on and running correctly.

Red (fixed or flashing). Indicates a pre-boot or that there is a PowerOn Self-Test (POST) error, preventing the system from booting.

Amber. Displayed during system reset, system lock, Standby mode
(Windows 98) or Suspend mode (Windows 95).

• *Hard disk drive activity LED.* Activated during POST and when the hard disk drive is being accessed.

HP Kayak XU700 Minitower Specifications and Characteristics

HP Kayak XU700 Minitower Specifications and Characteristics

Physical Characteristics

System Processing Unit	
Weight (Standard configuration as shipped, excl. keyboard and display)	14 kilograms (31.7 pounds).
Dimensions:	47.0 cm max. (D) by 21.0 cm (W) by 49.0 cm (H) (18.50 inches by 8.26 inches by 19.3 inches).
Footprint:	0.09 m ² (1.06 sq ft).

Electrical Specifications

	Total Rating		Peak (15 secs.)	Maximum per PCI Slots 32-bit 33 MHz	Maximum for AGP Slot ¹		
Parameter					Standard Connector	Extension	Total
Input voltage	100-127 V	200 -250 V	_	_	_	_	_
(Switch select)	VAC	Vac					
Input current (max)	5 A	2.5 A	_	_		_	_
Input frequency	50 to	60 Hz	_	_		_	_
Available power	320 W		_	100 W	V for PCI slots and AGP Pro slot		
Max current at +12 V	15	iΑ	15 A	0.5 A	1 A	4.2 A	5.2 A
Max current at -12 V	0.8	3 A	_	0.1 A	_	_	_
Max current at +3.3 V	28	ВА	_	7.6 A	6 A	7.6 A	13.6 A
Vddq ²	-	_	_	_			2 A
Max current at +5 V	30	I A	_	5 A			2 A
Max current at -5 V	0.0) A	_	_	-	_	_
Max current at +5V stdby 2 A combined with 3.3 V stdby		_	1.	875 A total on 3	.3 V stdby		

A maximum of 50 W can be drawn from the AGP Pro slot. The standard part of the AGP Pro connector supplies 25 W (max.) plus 25 W from the connector extension (25 W + 25 W = 50 W). Refer to page 30 for information about the AGP PRO Universal slot.

Only for I/O buffers.

If the overload protection in the power supply unit is triggered, all power is immediately cut. To reset the power supply unit, remove the power cord and then determine what caused the overload and remedy it. Reconnect the power cord, then reboot the PC Workstation. If an overload happens twice, then there is an undetected short circuit somewhere.

NOTE

When the PC Workstation is turned off with the power button on the front panel, the power consumption falls below the low power consumption (refer to the below table), but is not zero. The special on/off method used by this PC Workstation extends the lifetime of the power supply. To reach zero power consumption in "off" mode, either unplug the PC Workstation from the power outlet or use a power block with a switch.

Power Consumption and Cooling

The power consumption and acoustics given in the below table is valid for a standard configuration as shipped (one processor, 256 MB of memory, 320 W power supply, one hard disk drive, graphics card, LAN card).

All information in this section is based on primary power consumptions.

Power consumption (approximate values)	230 V / 50 Hz and 115 V / 60 Hz
Typical operatingSuspend (only on Windows 2000 models)	70 W - 238.8 Btu/h ¹ < 4 W - 13.6 Btu/h

^{1.} 1 W = 3.4121 Btu/h

Additional Component: Processor SCSI Hard disk drive with input/output access SCSI Hard disk without input/output access (idle) PCI card 50 W - 170.6 Btu/h 13 W - 78.4 Btu/h 16 W - 54.5 Btu/h 10 to 36 W - 64.1 Btu/h to 122.8 Btu/h

HP Kayak XU700 Minitower Specifications and Characteristics

Environmental Specifications

Environmental Specifications (System Processing Unit, with Hard Disk)					
Operating Temperature	+10 °C to +35 °C (+40 °F to +95 °F).				
Storage Temperature	-40 °C to +70°C (-40 °F to	+ 158 °F).			
Over Temperature Shutdown	+50°C (+122°F)				
Operating Humidity	15% to 80% (relative). ¹				
Storage Humidity	8% to 85% (relative). ¹				
Acoustic noise emission (as defined ISO 7779):	Sound Power	Sound Pressure			
OperatingOperating with hard disk accessOperating with floppy disk access	LwA <= 40.5 dB LwA <= 41.4 dB LwA <= 43.2 dB	$LpA \le 25.7 dB$ $LpA \le 26.5 dB$ $LpA \le 30.0 dB$			
Operating Altitude	10000 ft (3100m) max				
Storage Altitude	15000ft (4600m) max				

 $^{^{1}\}cdot$ non-condensing conditions.

Operating temperature and humidity ranges may vary depending upon the mass storage devices installed. High humidity levels can cause improper operation of disk drives. Low humidity levels can aggravate static electricity problems and cause excessive wear of the disk surface.

Power Saving and Ergonometry

Depending on the operating system, the following power management types are available:

- No sleeping state: Windows NT 4 (Full On and Off).
- APM: Windows 95 and Windows 98 SE APM (Full On, Suspend and Off).
- *ACPI*: Windows 98 SE ACPI and Windows 2000 (Full On, Standby, Hibernate, Off).

		Windows 2000	Windows 98 SE	Windows NT 4	Windows 95	
	Full On	Not Supported by	Supported	Supported	Supported	
A P M	Suspend	Windows 2000	Supported	Not Supported by Windows NT 4	Supported	
	Off		Supported	Supported	Supported	
A C P	Standby (S1 or S3)	Supported (implemented as S3, Suspend to RAM)	Supported (implemented as S1, suspend)	APM only Operating System		
ı	Hibernate (S4)	Supported	Not Supported			
	Off (\$5)	Supported	Supported			

Power Saving and Ergonometry

Power Saving and Ergonometry for APM Systems

	Full On	Suspend ¹	Off
Processor	Normal speed	Halted	Halted
Display	On	Blanked, < 5 W (typ)	Blanked, < 5 W (typ)
Hard disk drive	Normal speed	Halted	Halted
Power consumption	Supports up to 320 W	< 40 W (230V, 50 Hz) < 21 W (115V, 60 Hz)	(plugged in but turned off) < 5 W (average)
Resume events		Keyboard, network (RWU), modem, USB	Space bar or power button, RPO
Resume delay		A few seconds	Boot delay

^{1.} Not supported by Windows NT 4.

Power Saving Modes and Resume Events for ACPI Systems

	Full On (SO)	Suspend (S1)	Suspend to RAM (S3)	Suspend to Disk (S4)	Off (S5)
Processor	Normal speed	Halted	Off	Off	Off
Display	On	Blanked	Off	Off	Off
Hard Disk Drive	Normal speed	Halted	Off	Off	Off
Active Power Planes	VCC VCCAux	VCC VCCAux	Memory VCCAux	VCCAux	VCCAux
Power Consumption	Supports up to 320 W	< 40 W	< 10 W	< 10 W	< 10 W
Resume Events		Power button, LAN, Modem, USB, Scheduler, HP Start Key	Power button, LAN, Modem, Scheduler, HP Start Key	Power button, LAN, Modem, Scheduler, HP Start Key	Power button, HP Start Key
Resume Delay		Instantaneous	Instantaneous	BIOS boot delay	Regular boot delay

Power-On from Space-Bar

The *power-on from the space-bar* function is enabled provided that:

- The computer is connected to a Power-On keyboard (recognizable by the Power-On icon on the space bar).
- The function has not been disabled by setting SW-6 to **off** on the system board switches.

Soft Power Down

When the user requests the operating system to shut down, the environment is cleared, and the computer is powered off. *Soft Power Down* is available with Windows NT (when the Soft Power Down utility is used).

Documentation

The table below summarizes the availability of the documentation that is appropriate to the *HP Kayak XU700 PC Workstation*. Only selected publications are available in paper-based form. Most are available as printable files from the HP web site or the Information CD-ROM.

Title	Online at HP WWW Site (see address below)	Available on the Information CD-ROM	Paper-based
HP Desktop PCs Quick User's Guide	PDF file	No	A7185-XXXXX ¹
HP Kayak XU700 User's Guide	PDF file	Yes	No
HP Kayak XU700 Troubleshooting Guide	PDF file	Yes	No
HP Kayak XU700 Technical Reference Manual	PDF file	No	No
HP Kayak XU700 Service Handbook Chapter	PDF file	No	When available, chapter will be included in the fifth edition of the Service Handbook

XXXXX = includes language code.

Access HP World Wide Web Site

Additional online support documentation, BIOS upgrades and drivers are available from HP's World Wide Web site, at the following address:

World-Wide Web URL: http://www.hp.com/go/kayaksupport

After accessing the site, select HP Kayak XU700 PC Workstation.

Where to Find the Information

The table below summarizes information provided in the $HP\ Kayak\ XU700\ PC\ Workstation$ documentation set.

	Quick User's Guide User's Guide		Troubleshooting Service Guide ¹ Handboo		Technical Reference Manual
	1	Introducing t	he PC	l	l
Product features		Standard configuration.		Exploded view. Parts list.	Key features.
Product model numbers				Product range. CPL dates.	
Environmental	Setting up the PC. Working in comfort.				
Safety Warnings		Electrical, multimedia, safety, unpacking, removing & replacing cover.	Safety.		
Finding on-line information	HP Web sites.	Preloaded, HP Web sites.	HP Web sites.		HP Web sites, others.
Technical information	Basic details.	Basic details.			Advanced.
Formal documents	Certificate of Conformity. Software License agreement.				
		Using the	PC		
Connecting devices and turning on	Rear panel connectors, starting and stopping.				
BIOS		Basic details.	Updating and recovering.		Technical details. Memory maps.
Fields and their options within Setup		Basic details. Viewing <i>Setup</i> screen, using, passwords	Basic details.		Complete list.
Manageability		Power management, Software and drivers.			

	Quick User's Guide	User's Guide	Troubleshooting Guide ¹	Service Handbook	Technical Reference Manual
		Upgrading th	ie PC		
Opening the PC		Full description.			
Supported accessories				Full PN details	
Installing accessories		Processor(s), memory, accessory boards, mass storage devices.	Error messages, problem solving.		
Configuring devices		Installing devices	Installing devices.		
System board		Installing and removing, connectors and switch settings.	Switch settings.	Jumpers, switches and connectors.	Jumpers, switches and connectors. Chip-set details.
		Repairing th	e PC		
Troubleshooting	Basic.	Basic, MaxiLife, hardware diagnoses.	MaxiLife, hardware diagnoses and suggested solutions.	Service notes.	Advanced.
Power-On Self- Test routines (POST)		Basic details.	Error Messages, EMU and suggestions for corrective action.		Error codes and suggestions for corrective action. Order of tests.
Kayak diagnostic utility	e-DiagTools, CD-ROM recovery.	HP e-DiagTools, CD-ROM recovery.	HP e-DiagTools, CD-ROM recovery		Technical details.
		Peripheral De	evices		
Audio Accessories		Refer to Audio User's Guide for information on setting up and configuring audio accessories.	Refer to online version of Audio User's Guide for information on setting up and configuring audio accessories.		

	Quick User's Guide	User's Guide	Troubleshooting Guide ¹	Service Handbook	Technical Reference Manual
LAN Accessories		Refer to LAN Administrator's Guide for information on setting up and configuring LAN cards and systems.	Refer to online version (preloaded on hard disk) of LAN Administrator's Guide for information on setting up and configuring LAN cards and systems.		

^{1.} For address, "Access HP World Wide Web Site" on page 22.

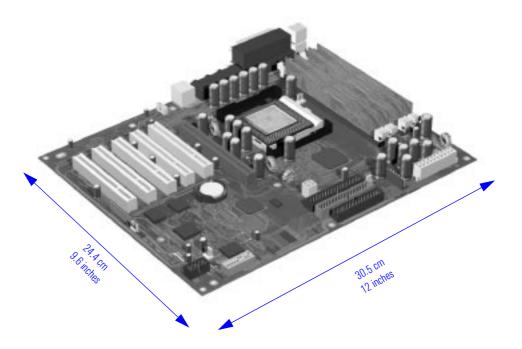
Documentation



System Board

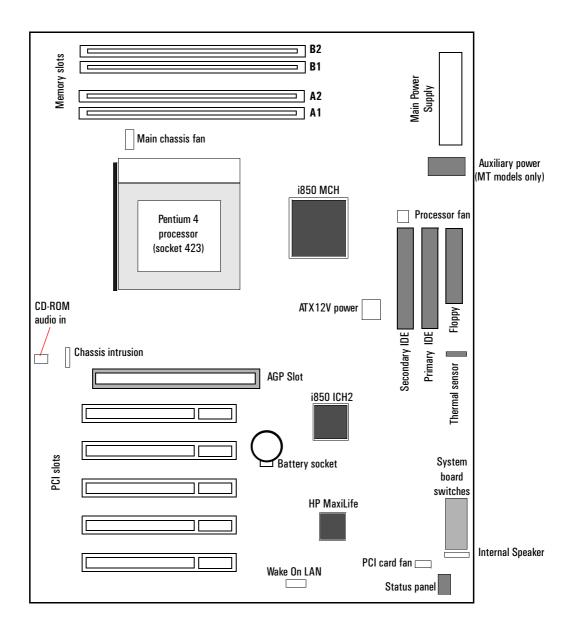
This chapter describes the components of the system board, taking in turn the components of the Memory Controller Hub (MCH), the Input/Output Controller Hub (ICH2), FirmWare Hub (FWH) and the System Bus.

The following diagram shows the $HP\ Kayak\ XU700\ PC\ Workstation$ system board in detail.

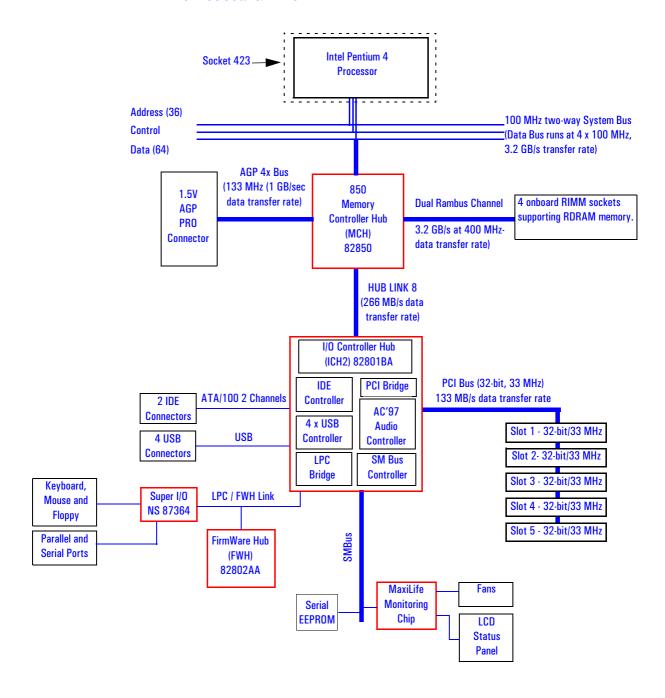


System Board Overview

The following diagram shows where the different chips and connectors are located on the system board.

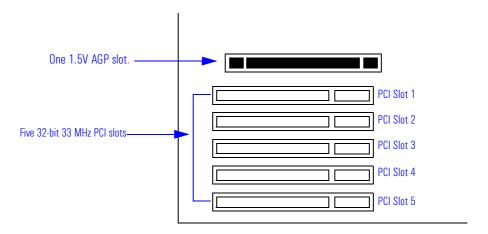


Architectural View

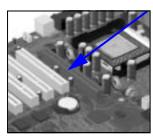


Accessory Board Slots

The following block diagram shows the position of the accessory board slots on the system board.



AGP Slot



Minitower models of the HP Kayak XU700 are equipped with a single AGP (Accelerated Graphics Port) graphics slot.

The AGP Pro Universal slot provides the ultimate graphics performance for high-end graphics cards, combining AGP 4X bandwidth (with data transfer rates up to $1056~\mathrm{MB/sec}$) with the ability to accept high-end graphics cards drawing up to $50~\mathrm{W}$ of power.

To accommodate AGP Pro cards, the AGP PRO slot connector is wider than the standard AGP 4X connector. Additional pins have been added at both ends of the connector to meet the increased power requirements of AGP Pro graphics cards.

An AGP Pro card may draw power either from the existing part of the AGP Pro connector, the extended part, or a combination of the two. In all cases, the maximum power that may be drawn by an AGP Pro card is limited to 50 W in the Minitower models. Power on the existing part of the connector is delivered on 5.0 V and 3.3 V rails. Power on the extension is delivered on the 12 V and 3.3 V rails.

Either standard AGP graphics cards or AGP Pro graphics cards drawing less than 50W of power can be used (below 25W a standard AGP connector may be used), with power being provided through 3.3 V, 5 V, or 12 V power rails.

NOTE

AGP Pro graphics cards drawing more than 50W ("high-power" AGP Pro cards) and AGP 3.3V graphics cards cannot be used in the Minitower's AGP slot.

The AGP Pro Universal slot is backwards compatible with both AGP 1x and 2.x modes (using 1.5 V signalling), and AGP 4x mode (where 1.5 V signalling is required).

The AGP interface and bus are explained on page 38.

PCI Slots



There is a total of five Peripheral Component Interconnect (PCI) 32-bit, 33 MHz connectors on the system board.

The PCI slots accept 3.3 V and 5 V PCI 32-bit 33 MHz cards, and Universal PCI cards (which are 3.3 V or 5 V compatible). Refer to the table on the following page for the different PCI board installations.

The maximum supported power consumption per slot is 25W, either from the 5V or the 3.3V supply and must respect the electrical specifications of the PCI 2.2 specification. Total power consumption for the PCI slots must not exceed 60 W.

The power consumption of each PCI board is automatically reported to the system through the two Presence Detect pins of each PCI slot. These pins code the following cases:

- No accessory board in the PCI slot.
- 7 W maximum PCI board in the PCI slot.
- 15 W maximum PCI board in the PCI slot.
- 25 W maximum PCI board in the PCI slot.

2 System Board

Accessory Board Slots

The following table shows the various PCI board installations for the different PCI slots:

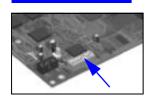
	PCI Card					
	3 3 V and 5 V			versal V compatible)		
PCI Slot	32-bit/ 33 MHz	64-bit/ 33 MHz		·bit/ or 66 MHz	_	bit/ or 66 MHz
Slots 1, 2, 3, 4 & 5 5 V, 32-bit/33 MHz	yes	yes ¹	yes	yes ²	yes ¹	yes ²

A 64-bit card can be installed in a 32-bit slot. However, this card will only operate in 32-bit mode.

The system board and BIOS support the PCI specification 2.2. This specification supports PCI-to-PCI bridges and multi-function PCI devices, and each of the five PCI slots have Master capabilities.

The PCI slots are connected to the ICH2 PCI 32-bit 33 MHz bus.

A 66 Mhz card can be installed in a 33 MHz slot. However, this card will only operate in 33 MHz mode.

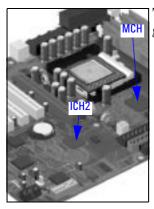


System Board Switches

There are ten system board switches used for configuration, numbered from 1 to 10. Some switches are reserved and should not be modified, otherwise it could lead to a system failure.

Switch	Default Position	Use
1-4	OFF	Reserved. Do Not change Default Settings
5	ON	Reserved. Do Not change Default Setting
6	ON	Enables keyboard power-on. OFF disables this option.
7	OFF	Enables normal modes. ON enables the BIOS recovery mode at next boot.
8	OFF	Retains CMOS memory. ON clears CMOS memory at next boot.
9	OFF	Enables User and System Administrator passwords. ON clears the passwords at next boot.
10	depends on chassis type	ON = minitower OFF = desktop

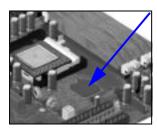
Chipset



The Intel[®] I850 chipset is a high-integration chipset designed for graphics/multimedia PC platforms and is comprised of the following:

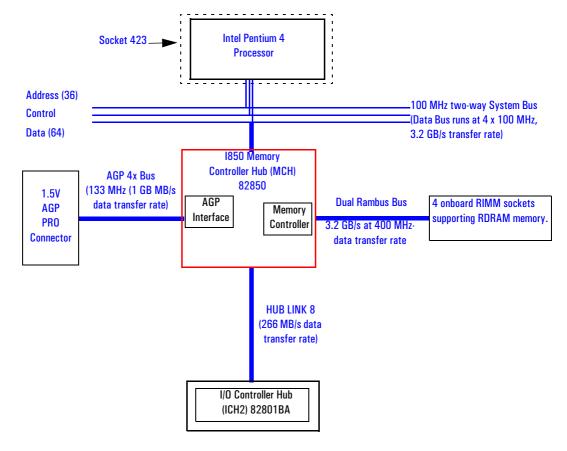
- The 82850 Memory Controller Hub (MCH) is a bridge between: the System bus, Dual Rambus bus (main memory), AGP 4x (graphic) bus and Hub Link 8-bit. The MCH chip feature is described in detail on page 35.
- \bullet The 82801BA Input/Output Controller Hub2 (ICH2) is a bridge between the following buses: the PCI bus (32-bits/33 MHz) and SMBus. In addition,
 - the ICH2 supports the integrated *IDE controller (Ultra ATA/100)*, Enhanced DMA controller, *USB controller, Interrupt controller, Low Pin Count (LPC) interface, FWH interface, ACPI Power Management Logic, AC'97 2.1 Compliant Link, AOL (Alert-On-LAN) and Real Time Clock (RTC) and CMOS.* The ICH2 is described in detail on page 42.
- The 82802AB Firmware Hub (FWH) stores system BIOS and SCSI BIOS, nonvolatile memory component. In addition, the FWH contains an Intel® Random Number Generator (RNG). The RNG provides random numbers to enable fundamental security building blocks for stronger encryption, digital signing and security protocols for the PC Workstation. The FWH is described in detail on page 54.

Memory Controller Hub (82850)



The MCH Host Bridge/Controller is contained in a 615-pin Organic Land Grid Array (OLGA) package and is the bridge between the System bus, Dual Rambus bus (main memory), AGP 4x (graphic) bus and Hub Link 8-bit.

The following figure shows an example of the system block diagram using the MCH.



2 System Board

Memory Controller Hub (82850)

The following table shows the features that are available in the MCH Host Bridge/Controller.

Feature	Feature
 Processor/System Bus: Supports on Pentium 4 processor at: 100 MHz System Bus frequency (400 MHz Data Bus). Provides an 8-deep In-Order Queue supporting up to eight outstanding transaction requests on the System bus. Desktop optimized AGTL + bus driver technology with integrated AGTL + termination resistors. Support for 32-bit System bus address. 	 Accelerated Graphics Port (AGP) Interface: Single 1.5V AGP PRO connector. AGP Rev 2.0 compliant, including AGP 4x data transfers and 2x/4x Fast Write protocol. AGP 1.5V connector support with 1.5 V signalling only. AGP PIPE# or SBA initiated accesses to DRAM is not snooped AGP FRAME initiated accesses to DRAM are snooped (snooper identifies that data is coherent in cache memory). Hierarchical PCI configuration mechanism. Delayed transaction support for AGP-to-DRAM reads that cannot be serviced immediately.
Memory Controller.	
Direct Rambus:	
 Dual Direct Rambus Channels operating in lock-step (both channels must be populated with a memory module). Supporting 300 MHz or 400 MHz. RDRAM 128 Mb, 256 Mb devices. Minimum upgrade increment of 32 MB using 128 Mbit DRAM technology. Up to 64 Direct Rambus devices. Dual channel maximum memory array size is: 1 GB using 128 Mbit DRAM technology. 2 GB using 256 Mbit DRAM technology. Up to 8 simultaneous open pages: 1 KByte page size support for 128 Mbit and 256 Mbit RDRAM devices. 2 KByte page size support for 256 Mbit RDRAM devices. 	
 Hub Link 8-bit Interface to ICH2: High-speed interconnect between the MCH and ICH2 (266 MB/sec). 	

Feature	Feature
 Power management: SMRAM space re-mapping to A0000h - BFFFFh (128 KB). Extended SMRAM space above 256 MB, additional 128 K, 256 K, 512 K, 1 MB TSEG from Top of Memory, cacheable (cacheability controlled by processor). Suspend to RAM. ACPI Rev. 1.0 compliant power management. APM Rev. 1.2 compliant power management. Power-managed states are supported for up to two processors. 	 Arbitration: Distributed Arbitration Model for Optimum Concurrency Support. Concurrent operations of System, hub interface, AGP and memory buses supported via a dedicated arbitration and data buffering logic.
• 615 OLGA MCH package.	Input/Output Device Support: □ Input/Output Controller Hub (ICH2). □ PCI 64 Hub (P64H).

MCH Interface

The MCH interface provides bus control signals and address paths via the Hub Link 8-bit access to the ICH2 for transfers between the processor on the system bus, Dual Rambus bus and AGP 4x bus.

The MCH supports 32-bit host addresses, allowing the processor to address a space of 4GB. It also provides an 8-deep In-Order Queue supporting up to eight outstanding transaction requests on the system bus.

Host-initiated input/output signals are positively decoded to AGP or MCH configuration space and subtractively decoded to Hub Link 8-bit interface. Host-initiated memory cycles are positively decoded to AGP or RDRAM, and are again subtractively decoded to Hub Link 8-bit interface.

AGP semantic memory accesses initiated from AGP to DRAM do not require a snoop cycle (not snooped) on the System bus, since the coherency of data for that particular memory range will be maintained by the software. However, memory accesses initiated from AGP using PCI Semantics and accesses from Hub Link interface to RDRAM do require a snoop cycle on the System bus.

Memory access whose addresses are within the AGP aperture are translated using the AGP address translation table, regardless of the originating interface.

Write accesses from Hub Link interface to the AGP are supported.

Memory Controller Hub (82850)

The MCH supports one Pentium 4 processor at an FSB frequency of 100MHz using AGTL+ signalling. Refer to page 56 for a description of the System bus.

Accelerated Graphics Port (AGP) Bus Interface

A controller for the Universal AGP (Accelerated Graphics Port) Pro slot is integrated in the MCH. The AGP Bus interface is compatible with the Accelerated Graphics Port Specification, Rev 2.0, operating at 133 MHz, and supporting up to 1 GB/sec data transfer rates. The MCH supports only a synchronous AGP interface, coupling to the System bus frequency.

AGP 4x Bus

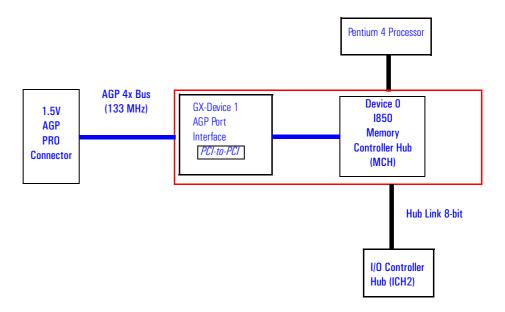
The AGP bus is a dedicated bus for the graphics subsystem, which meets the needs of high quality 3D graphics applications. It has a direct link to the MCH.

The AGP bus is based upon a 66 MHz, 32-bit PCI bus architecture, to which several signal groups have been added to provide AGP-specific control and transfer mechanisms.

AGP specific transactions always use pipelining. This control mechanism increases the bus efficiency for data transfer. Sideband Addressing (SBA) may also be used by AGP transaction requests which further increases the bus efficiency for data transfer. The supported modes are detailed below:

- FRAME-based AGP. Only the PCI semantics are: 66 MHz, 32-bit, 1.5 V, 266 MB/s peak transfer rate.
- AGP 1X with pipelining, sideband addressing can be added: uses 66 MHz, 32-bit, 1.5 V, increased bus efficiency, 266 MB/s peak transfer rate.
- AGP 2X with pipelining, sideband addressing can be added: 66 MHz double clocked, 32-bit, 1.5 V, 533 MB/s peak transfer rate.
- AGP 4X with pipelining, sideband addressing can be added: 133 MHz double clocked, 32-bit, 1.5 V, increased bus efficiency, 1066 MB/s peak transfer rate

AGP PCI Bus Implementation



Main Memory Controller

The main memory controller is integrated in the MCH supporting two primary rambus channels (A and B).

DRAM Interface

The MCH provides optional System bus error checking for data, address, request and response signals. Only 400 MHz Direct Rambus devices are supported in any of 128 or 256 Mbit technology. 128 Mbit RDRAM uses page sizes of 1 kbytes, while 256 Mbit devices target 1 kbyte or 2 kbyte pages.

A maximum number of 32 Rambus devices (128 Mbit technology implies 1 GB maximum in 32 MB increments, 256 Mbit technology implies 2 GB maximum in 64 MB increments) are supported on the Direct Rambus channel without external logic.

The MCH also provides optional data integrity features including ECC in the memory array. During DRAM writes, ECC is generated on a QWord (64 bit) basis. During DRAM reads, the MCH supports multiple-bit error detection and single-bit error correction when the ECC mode is enabled.

Memory Controller Hub (82850)

MCH will scrub single bit errors by writing the corrected value back into DRAM for all reads when hardware scrubbing is enabled. This, however does not include reads launched in order to satisfy an AGP aperture transaction.

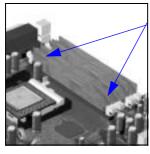
ECC can only be enabled when all RDRAM devices are populated in a system that supports the extra two data bits used to store the ECC code.

Dual Rambus Bus

The Dual Rambus bus is comprised of 16×2 bits of data information, and 8 bits of Error Correcting Code (ECC). The bus is connected to the RIMM memory slots and to the MCH chip supporting two Dual Rambus channels (A and B).

Both channels run at 300 or 400 MHz supporting up to 32 rambus devices per channel. The maximum available data bandwidth is 3.2 GB/s at 400 MHz.

The configuration of both primary rambus channels must be symmetrical – the memory configuration on channel A must be identical to the memory configuration on channel B. This means the memory must be installed in identical pairs.



RIMM Memory Slots

The *HP Kayak XU700 PC Workstation* has four RIMM memory sockets, RIMM A1, RIMM A2, RIMM B1, RIMM B2, for installing two or four RDRAM memory modules.

Each pair of memory sockets must contain identical memory modules (identical in size, speed and type). That is, sockets **A1** and **B1** must contain identical modules, and sockets **A2** and **B2** must contain identical modules (or continuity modules).

If only two RDRAM modules are installed, use the sockets marked **A1** and **B1**. The other two sockets (**A2** and **B2**) must contain continuity modules.

If only Each DIMM socket is connected to the SMBus and is described on page 49.

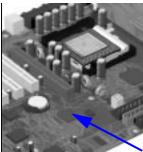
Read/Write Buffers

The MCH defines a data buffering scheme to support the required level of concurrent operations and provide adequate sustained bandwidth between the DRAM subsystem and all other system interfaces (CPU, AGP and PCI).

System Clocking

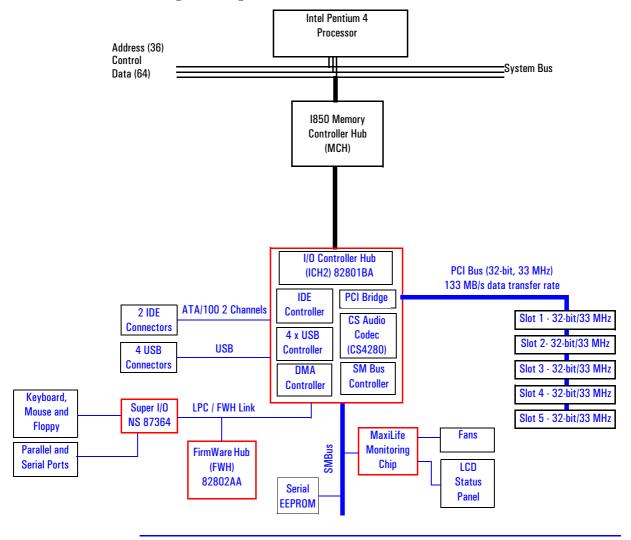
The MCH operates the System interface at 100 MHz or, PCI at 33 MHz and AGP at 66/133 MHz. Coupling between all interfaces and internal logic is done in a synchronous manner. The clocking scheme uses an external clock synthesizer (which produces reference clocks for the host, AGP and PCI interfaces).

The Input/Output Controller Hub 2 (82801BA)



The ICH2 is encapsulated in a 360-pin Enhanced Ball Grid Array (EBGA) package and is located on the system board just underneath the AGP connector. It provides the interface between the PCI bridge (PCI Rev. 2.2 compliant with support for 32-bit 33 MHz PCI operations), PCI-to-LPC (Low Pin Count) bridge, IDE controller, USB controller, SMBus controller and Audio Codec '97 controller.

The ICH2 functions and capabilities are discussed in detail later on in this section. The following figure shows an example of the system block diagram using the ICH2.



The following table shows the available ICH2 features.

Feature	Feature
 Multi-function PCI Bus Interface: PCI at 32-bit 33 MHz. PCI Rev 2.2 Specification. 133 Mbyte/sec data transfer rate. 	 Enhanced DMA Controller: Two 82C37 DMA controllers. PCI DMA with 2 PC/PCI Channels in pairs. LPC DMA.
☐ Master PCI Device Support for up to five devices.	DMA Collection Buffer to provide Type-F DMA performance for all DMA channels.
USB, supporting:	Interrupt Controller:
USB revision 1.1 compliant.UHCI Implementation with four USB Ports for serial	☐ Two cascaded 82C59 controllers.☐ Integrated I/O APIC capability.
transfers at12 or 1.5 Mbit/sec. ☐ Wake-up from sleeping states.	15 Interrupt support in 8259 Mode, 24 supported in I/O APIC mode.
☐ Legacy keyboard/mouse software.	☐ Serial Interrupt Protocol.
Power Management Logic:	Integrated IDE Controller:
 ACPI 1.0 compliant. Support for APM-based legacy power management for non-ACPI implementations. ACPI defined power states (S1, S3, S4, S5). ACPI power management timer. SMI generation. 	☐ Independent Timing of up to four drives. ☐ Ultra ATA/100 Mode (100 Mbytes/sec). ☐ Ultra ATA/66 Mode (66 Mbytes/sec). ☐ Ultra ATA/33 Mode (33 Mbytes/sec). ☐ PIO Mode 4 transfers up to 14 Mbytes/sec. ☐ Separate IDE connections for Primary and Secondary cables.
 □ All registers readable/restorable for proper resume from 0 V suspend states. □ PCI PME#. 	☐ Integrated 16 x 32-bit buffer for IDE PCI Burst transfers. ☐ Write Ping-Pong Buffer for faster write performances.
Real-Time Clock, supporting:	System TCO Reduction Circuits:
256-byte battery-backed CMOS RAM.Hardware implementation to indicate Century Rollover.	 □ Timers to Generate SMI# and Reset Upon. □ Timers to Detect Improper Processor Reset. □ Integrated Processor Frequency Strap Logic.
Timers Based on 82C54:	• SMBus
☐ System Timer, Refresh Request, Speaker Tone Output.	 ☐ Host Interface allows processor to communicate via SMBus. ☐ Compatible with 2-wire I²C bus.
System Timer, Refresh Request, Speaker Tone Output.	GPI0:
	☐ TTL, Open-Drain, Inversion.
Firmware Hub (FWH) interface.	• 3.3 V operation with 5 V Tolerant Buffers for IDE and PCI signals.
241 BGA Package.	Alert-On-LAN (AOL) support.

The Input/Output Controller Hub 2 (82801BA)

ICH2 Architecture

The ICH2 interface architecture ensures that the I/O subsystems, both PCI and the integrated input/output features (for example: IDE, AC'97 and USB) receive the adequate bandwidths.

To achieve this, by placing the I/O bridge directly on the ICH2 interface, and no longer on the PCI bus, the ICH2 architecture ensures that both the input/output functions integrated into the ICH2 and the PCI peripherals obtain the bandwidth necessary for peak performance.

ICH2 PCI Bus Interface

The ICH2 PCI provides the interface to a PCI bus interface operating at 33 MHz. This interface implementation is compliant with PCI Rev 2.2 Specification, supporting up to five external PCI masters in addition to the ICH2 requests. The PCI bus can reach a data transfer rate of 133 MBytes/sec. The maximum PCI burst transfer can be between 256 bytes and 4 KB. It also supports advanced snooping for PCI master bursting, and provides a pre-fetch mechanism dedicated for IDE read.

Refer to the table page 59 for ICH2 interrupts.

SMBus Controller

The System Management (SM) bus is a two-wire serial bus which runs at a maximum of (100 kHz). The SMBus Host interface allows the processor to communicate with SMBus slaves and an SMBus Slave interface that allows external masters to activate power management events. The bus connects to sensor devices that monitor some of the hardware functions of the system board, both during system boot and run-time.

Refer to page 47 for a description of the devices on the SMBus, or to page 50 for information on the MaxiLife ASIC.

Low Pin Count Interface The ICH2 implements the LPC interface 1.0 specification.

Enhanced USB Controller The USB (Universal Serial Bus) controller provides enhanced support for the Universal Host Controller Interface (UHCI). This includes support that allows legacy software to use a USB-based keyboard and mouse. The USB supports four stacked connectors on the back panel. These ports are built into the ICH2, as standard USB ports.

The ICH2 is USB revision 1.1 compliant.

USB works only if the USB interface has been enabled within the HP Setup program. Currently, only the Microsoft Windows 95 SR2.1, Windows 98 and Windows 2000 operating systems provide support for the USB.

AC'97 Controller

This is the single-chip CS4299 audio controller that provides full audio features for the Kayak XU700.

Refer to page 46 for information about the CS4299 audio solution.

IDE Controller

The IDE controller is implemented as part of the ICH2 chip and has PCI-Master capability. Two independent ATA/100 IDE channels are provided with two connectors per channel. Two IDE devices (one master and one slave) can be connected per channel. In order to guarantee data transfer integrity, Ultra-ATA cables must be used for Ultra-ATA modes (Ultra-ATA/33, Ultra-ATA/66 and Ultra-ATA/100).

The PIO IDE transfers of up to 14 Mbytes/sec and Bus Master IDE transfer rates of up to 66 Mbytes/sec are supported. The IDE controller integrates 16 x 32-bit buffers for optimal transfers.

It is possible to mix a fast and a slow device, such as a hard disk drive and a CD-ROM, on the same channel without affecting the performance of the fast device. The BIOS automatically determines the fastest configuration that each device supports.

DMA Controller

The seven-channel DMA controller incorporates the functionality of two 82C37 DMA controllers. Channels 0 to 3 are for 8-bit count-by-byte transfers, while channels 5 to 7 are for 16-bit count-by-word transfers (refer to table on page 93 for allocated DMA channel allocations). Any two of the seven DMA channels can be programmed to support fast Type-F transfers.

The ICH2 DMA controller supports the LPC (Low Pin Count) DMA. Single, Demand, Verify and Incremental modes are supported on the LPC interface. Channels 0-3 are 8-bit, while channels 5-7 are 16-bit. Channel 4 is reserved as a generic bus master request.

Interrupt Controller

The Interrupt controller is equivalent in function to the two 82C59 interrupt controllers. The two interrupt controllers are cascaded so that 14 external and two internal interrupts are possible. In addition, the ICH2 supports a serial interrupt scheme and also implements the I/O APIC controller. A table on page 59 shows how the master and slave controllers are connected.

The Input/Output Controller Hub 2 (82801BA)

Timer/Counter Block

The timer/counter block contains three counters that are equivalent in function to those found in one 82C54 programmable interval counter/timer. These three counters are combined to provide the system timer function. and speaker tone. The 14.318 MHz oscillator input provides the clock source for these three counters.

Interrupt Controller

Advanced Programmable Incorporated in the ICH2, the APIC can be used in either single-processor or multi-processor systems, while the standard interrupt controller supports only single-processor systems.

Real Time Clock

The RTC is 146818A-compatible, with 256 bytes of CMOS. The RTC performs two key functions: keeping track of the time of day and storing system data.

The RTC operates on a 32.768 kHz crystal and a separate 3V lithium battery that provides up to 7 years of protection for an unplugged system. It also supports two lockable memory ranges. By setting bits in the configuration space, two 8-byte ranges can be locked to read and write accesses. This prevents unauthorized reading of passwords or other security information. Another feature is a date alarm allowing for a schedule wake-up event up to 30 days in advance.

Enhanced Power Management

The ICH2's power management functions include enhanced clock control, local and global monitoring support for 14 individual devices, and various low-power (suspend) states. A hardware-based thermal management circuit permits software-independent entry points for low-power states.

The ICH2 includes full support for the Advanced Configuration and Power Interface (ACPI) specifications.

Crystal CS4299 Integrated PCI Audio

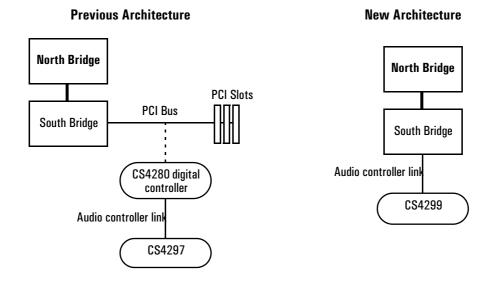
Based on the earlier Crystal audio controller, the CS4299 extends these features to include, among many other enhancements, PC'98 and PC'99 compliancy for multimedia desktops requiring high quality audio.

Features of the CS4299 include:

- AC'97 2.1 compatibility
- Industry leading mixed signal technology
- 20-bit stereo digital-to-analog converter and 18-bit analog-to-digital converter

- High quality pseudo differential CD input
- Mono microphone input
- An analog line-level stereo inputs for LINE IN
- Stereo line level output
- Meets or exceeds Microsoft's PC'98 and PC'99 audio performance requirements.

The CS4299 introduces a new architecture that is different from the one used with the CS4280-CS4297 pair.



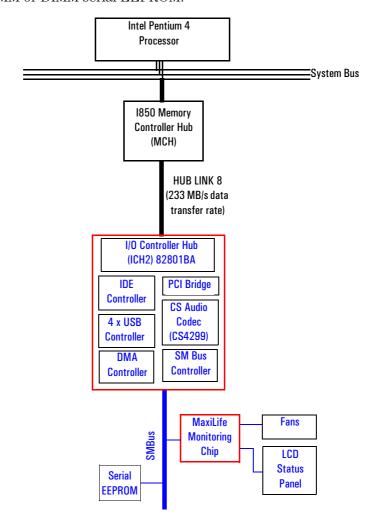
Devices on the SMBus

The SMBus is a subset of the I^2C bus. It is a two-wired serial bus which runs at a maximum speed of 100 kHz. It is used to monitor some of the hardware functions of the system board (such as voltage levels, temperature, fan speed, memory presence and type), both at system boot and during normal run-time. It is controlled by the SMBus controller located in the ICH2.

The Input/Output Controller Hub 2 (82801BA)

The following devices are connected to the SMBus:

- LCD status panel.
- One Serial EEPROM MaxiLife (also includes backup values of CMOS settings).
- PCI slot 5, thus being ready for Alert-On LAN (AOL) from a hardware level
- ICH2 SMBus Master Controller 100 kHz maximum.
- MaxiLife for hardware management, bus master controller.
- One LM75 thermal sensor on the system board.
- One ADM1024 hardware monitoring sensor.
- RIMM or DIMM serial EEPROM.



ICH2 SMBus Master Controller

The ICH2 provides a processor-to-SMBus controller. All access performed to the SMBus is done through the ICH2 SMBus interface. Typically, the processor has access to all the devices connected to the SMBus.

DIMM Sockets

Each DIMM socket is connected to the SMBus. The 168-pin DIMM modules include a 256 byte $\rm I^2C$ Serial EEPROM. The first 128 bytes contain general information, including the DRAM chips' manufacturer's name, DIMM speed rating, DIMM type, etc. The second 128 bytes of the Serial EEPROM can be used to store data online.

RIMM Sockets

Each RIMM socket is connected to the SMBus. The 168-pin RIMM modules include a 256 byte $\rm I^2C$ Serial EEPROM. The first 128 bytes contain general information, including the DRAM chips' manufacturer's name, RIMM speed rating, RIMM type, etc. The second 128 bytes of the Serial EEPROM can be used to store data online.

ADM1024

The ADM1024 chip is a hardware monitoring sensor dedicated to the processor temperature. This chip uses the thermal diodes integrated into each processor cartridge and makes the temperature information available through the SMBus. It also monitors processor power supply voltages.

Serial EEPROM

This is the non-volatile memory which holds the default values for the CMOS memory (in the event of battery failure). When installing a new system board, the Serial EEPROM will have a blank serial number field. This will be detected automatically by the BIOS, which will then prompt the user for the serial number which is printed on the identification label on the back of the PC Workstation.

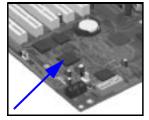
The computer uses 16KBytes of Serial EEPROM implemented within two chips. Serial EEPROM is ROM in which one byte at a time can be returned to its unprogrammed state by the application of appropriate electrical signals. In effect, it can be made to behave like very slow, non-volatile RAM. It is used for storing the tatoo string, the serial number, and the parameter settings for the *Setup* program as well as MaxiLife firmware.

LM75 Temperature Sensor

The LM75 temperature sensor and alarm are located on the system board. The sensor is used to measure the temperature in various areas of the system board. This information is used to regulate fans.

The Input/Output Controller Hub 2 (82801BA)

HP MaxiLife Hardware Monitoring Chip



MaxiLife is a hardware monitoring chip which is resident on the system board. Its responsibility includes On/Off and reset control, status panel management (Lock button, LEDs), hardware monitoring (temperature and voltage), early diagnostics (CPU, memory, PLLs, boot start), run-time diagnostics (CPU errors), fan speed regulation, and other miscellaneous functions (such as special OK/FAIL symbols based on a smiling face).

The integrated microprocessor includes a Synopsys cell based on Dallas "8052" equivalent, a 2 KB boot ROM, 256 bytes of data RAM, an I²C cell, an Analog-to-Digital (ADC) with 5 entries, and an additional glue logic for interrupt control, fan regulation, and a status panel control.

MaxiLife downloads its code in 96 milliseconds from an I²C serial EEPROM. The total firmware (MaxiLife 8051-code, running in RAM) size is 14 KB. As it exceeds the 2 KB program RAM space, a paging mechanism will swap code as it is required, based on a 512 byte buffer. The first 2 KB pages of firmware code is critical because it controls the initial power on/reset to boot the system. This initial page is checked with a null-checksum test and the presence of MaxiLife markers (located just below the 2 KB limit).

MaxiLife is not accessible in I/O space or memory space of the system platform, but only through the SMBUS (which is a sub-set of the I²C bus), via the ICH2. Its I²C cell may operate either in Slave or Master mode, switched by firmware, or automatically in the event of 'Arbitration' loss.

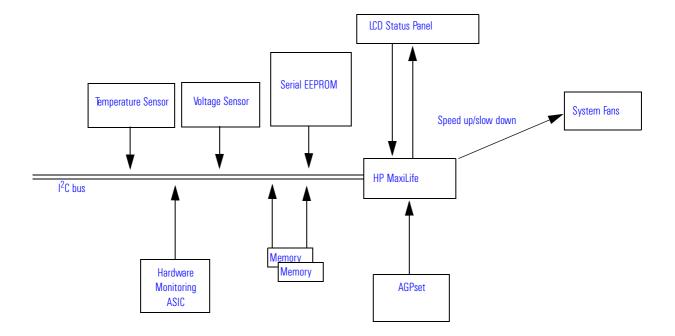
As a monitoring chip, MaxiLife reports critical errors at start-up, and is therefore powered by Vstandby (3.3V) power. For MaxiLife to work, the PC Workstation must be connected to a grounded outlet. This enables the PC Workstation's hardware monitoring chip to be active, even if the system has been powered off.

Test Sequence and Error Messages

Refer to <u>"MaxiLife Test Sequence and Error Messages" on page 97</u> for detailed information about the different test sequences and error messages

MaxiLife Architecture

The MaxiLife chip continuously monitors temperature and voltage sensors located in critical regions on the system board. This chip receives data about the various system components via a dedicated I^2C bus, which is a reliable communications bus to control the integrated circuit boards.



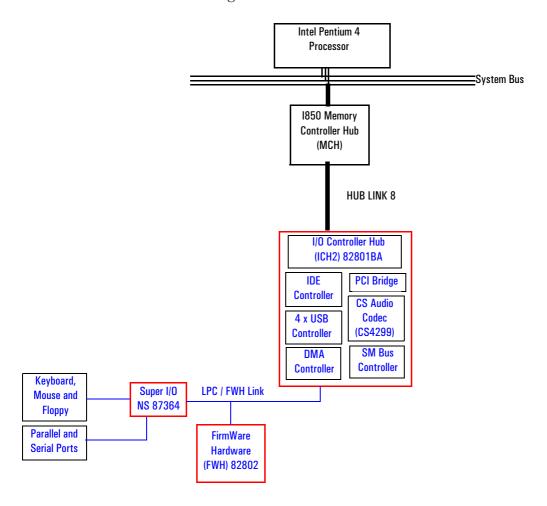
NOTE

MaxiLife is powered by VSTBY. This means that it is functional as soon as the power cord is plugged in.

The Input/Output Controller Hub 2 (82801BA)

Devices on the Low Pin Count Bus

The following devices are connected to the LPC bus.



The Super I/O Controller (NS 87364)

The *Super I/O* chip (NS 87364) provides the control for two FDD devices, two serial ports, one bidirectional multi-mode parallel port and a keyboard and mouse controller.

Device	Index	Data
Super I/O	2Eh	2Fh

Serial / Parallel Communications Ports

The 9-pin serial ports (whose pin layouts are depicted on <u>page 123</u>) support RS-232-C and are buffered by 16550A UARTs, with 16-Byte FIFOs. They can be programmed as COM1, COM2, COM3, COM4, or disabled.

The 25-pin parallel port (also depicted on page 124) is Centronics compatible, supporting IEEE 1284. It can be programmed as LPT1, LPT2, or disabled. It can operate in the four following modes:

- ☐ Standard mode (PC/XT, PC/AT, and PS/2 compatible).
- ☐ Bidirectional mode (PC/XT, PC/AT, and PS/2 compatible).
- ☐ Enhanced mode (enhanced parallel port, EPP, compatible).
- ☐ High speed mode (MS/HP extended capabilities port, ECP, compatible).

FDC

The integrated *floppy disk controller* (FDC) supports any combination of two of the following: tape drives, 3.5-inch flexible disk drives, 5.25-inch flexible disk drives. It is software and register-compatible with the 82077AA, and 100% IBM-compatible. It has an A and B drive-swapping capability and a non-burst DMA option.

Keyboard and Mouse Controller

The computer has an 8042-based keyboard and mouse controller. The connector pin layouts are shown on page 122.

FirmWare Hub (82802AB)

The FWH (also known as flash memory) is connected to the LPC bus. It contains 4 Mbit (512 kB) of flash memory.

The hardware features of the FWH include: a Random Number Generator (RNG), five General Purpose Inputs (GPI), register-based block locking and hardware-based locking. An integrated combination of logic features and non-volatile memory enables better protection for the storage and update of system code and data, adds flexibility through additional GPIs, and allows for quicker introduction of security/manageability features.

The following table shows the available FWH features.

Feature	Feature
 Platform Compatibility: Enables security-enhanced platform infrastructure. Part of the Intel I840 chipset. FirmWare Hub Interface Mode: Five signal communication interface supporting x8 reads and writes. Register-based read and write protection for each code/data storage blocks. Five additional GPIs for system design and flexibility. A hardware RNG (Random Number Generator). Integrated CUI (Command User Interface) for requesting access to locking, programming and erasing options. It also handles requests for data residing in status, ID and block lock registers. 	 Two Configurable Interfaces: FirmWare Hub interface for system operation. Address/Address Multiplexed (A/A Mux) interface. 4 Mbits of Flash Memory for system code/data non-volatile storage: Symmetrically blocked, 64 Kbyte memory sections. Automated byte program and block erase through an integrated WSM (Write State Machine).
 Operates with 33 MHz PCI clock and 3.3 V input/output. A/A Mux Interface/Mode, supporting: 	Power Supply Specifications:
 11-pin multiplexed address and 8-pin data I/O interface. Fast on-board or out-of-system programming. 	 Vcc: 3.3 V +/- 0.3 V. Vpp: 3.3 V and 12 V for fast programming, 80 ns.
● Industry Standard Packages: □ 40L TSOP or 32L PLCC.	Case Temperature Operating Range.

The FWH includes two hardware interfaces:

- FirmWare Hub interface.
- Address/Address Multiplexed (A/A Mux) interface.

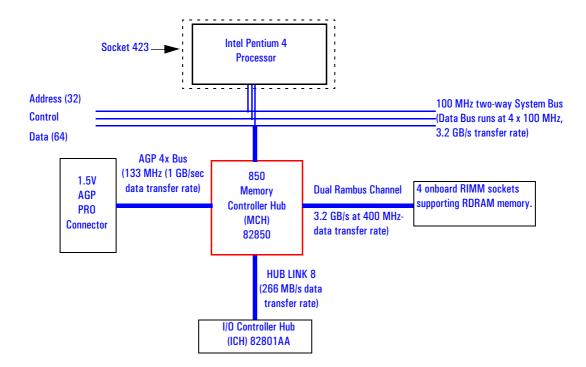
The IC (Interface Configuration) pin on the FWH provides the control between these interfaces. The interface mode needs to be selected prior to power-up or before return from reset (RST# or INIT# low to high transition).

The FWH interface works with the ICH2 during system operation, while the A/A Mux interface is designed as a programming interface for component pre-programming.

An internal CUI (Command User Interface) serves as the control center between the FWH and A/A Mux interfaces, and internal operation of the non-volatile memory. A valid command sequence written to the CUI initiates device automation. An internal WSM (Write State Machine) automatically executes the algorithms and timings necessary for block erase and program operations.

System Bus

The system bus of the Pentium 4 processor is implemented in the GTL (Gunning Transceiver Logic)+ technology. This technology features opendrain signal drivers that are pulled up through resistors at bus extremities to the operating voltage of the processor core. These resistors also act as bus terminators, and are integrated in the processor and in the 82850 MCH.



The supported operating frequency of the GTL+ bus for the Pentium 4 is 100 MHz. The width of the data bus is 64 bits, while the width of the address is 32 bits. Data bus transfers occur at four times the system bus, at 400 MHz. Along with the operating frequencies, the processor voltage is set automatically.

The control signals of the system bus allow the implementation of a "split-transaction" bus protocol. This allows the Pentium 4 processor to send its request (for example, for the contents of a given memory address) and then to release the bus, rather than waiting for the result, thereby allowing it to

accept another request. The MCH, as target device, then requests the bus again when it is ready to respond, and sends the requested data packet. Up to four transactions are allowed to be outstanding at any given time.

Intel Pentium 4 Processor

The Pentium 4 processor has several features that enhance performance:

- Data bus frequency of 400 MHz.
- Dual Independent Bus architecture, which combines a dedicated 64-bit L2 cache bus (supporting 256 KB) plus a 64-bit system bus that enables multiple simultaneous transactions.
- MMX2 technology, which gives higher performance for media, communications and 3D applications.
- Dynamic execution to speed up software performance.
- Internet Streaming SIMD Extensions 2 (SSE2) for enhanced floating point and 3D application performance.
- Uses multiple low-power states, such as AutoHALT, Stop-Grant, Sleep and Deep Sleep to conserve power during idle times.

The Pentium 4 processor is packaged in a pin grid array (PGA) that fits into a PGA423 socket (423-pin Zero Insertion Force or ZIF socket).

Processor Clock

The 100 MHz System Bus clock is provided by a PLL. The processor core clock is derived from the System Bus by applying a "ratio". This ratio is fixed in the processor. The processor then applies this ratio to the System bus clock to generate its CPU core frequency.

Bus Frequencies

There is a 14.318 MHz crystal oscillator on the system board. This frequency is multiplied to 133 MHz by a phase-locked loop. This is further scaled by an internal clock multiplier within the processor.

The bus frequency and the processor voltage are set automatically.

Voltage Regulation Module (VRM)

One VRM is integrated on the system board complying with VRM specification rev. 9.0. High-current and low voltage processors are supported.

The processor requires a dedicated power voltage to supply the CPU core and L2 cache. The processor codes through Voltage Identification (VID) pins with a required voltage level of $1.30~\rm V$ to $2.05~\rm V$. The VID set is decoded

System Bus

by the VRM on the system board that in return supplies the required power voltage to the processor. It should be noted, however, that voltage may vary from one processor model to another.

Cache Memory

The Pentium 4 integrates the following cache memories on the same die as the processor cache:

- A trace instruction and L1 data cache. The trace cache is 4-way set associative.
- A 256KB L2 cache. The L2 cache is 8-way associative.

The amount of cache memory is set by Intel at the time of manufacture, and cannot be changed.

Assigned Device Interrupts

Input/Output Controller Hub Interrupts

Device	Reference	REQ/G	ID IDSEL		Cl	nip-set Interr	upt Connecti	on
Device	Name	NT	טו	AD[xx]	INTA	INTB	INTC	INTD
AC'97 Audio Controller	CS4280	4 (ICH2)	5	21	_	А	_	_
USB Controller	_	_	_	_	А	_	_	_
AGP slot	J34	_	0	16	А	В	_	_
PCI 32-bit slot #1	J37	1 (ICH2)	6	22	С	D	А	В
PCI 32-bit slot #2	J38	0 (ICH2)	8	24	А	В	С	D
PCI 32-bit slot #5 (LAN card)	J42	5 (ICH2)	11	27	В	С	D	А

PCI 64-bit Hub Interrupts

Device	Reference	REQ/G ID		REQ/G ID	Reference REQ/G	IDSEL			Inte	rrupt	Requ	ests (I	RQ)		
Device	Name	NT	10	AD[xx]	0	1	2	3	4	5	6	7	8		
Ultra-wide SCSI U160 Controller	AIC-7892	2 (P64H)	9	25	_	_	_	-	_	_	_	_	Α		
PCI 32-bit slot #3	J39	1 (P64H)	4	20	_	_	_	-	Α	В	С	D	_		
PCI 32-bit slot #4	J40	0 (P64H)	7	23	Α	В	С	D	_	_	_	_	_		

Interrupt Controllers

The system has an Interrupt controller which is equivalent in function to that of two 82C59 interrupt controllers. The following table shows how the interrupts are connected to the APIC controller. The Interrupt Requests (IRQ) are numbered sequentially, starting with the master controller, and followed by the slave (both of 82C59 type).

Although the *Setup* program can be used to change some of the settings, the following address map is not completely BIOS dependent, but is determined partly by the operating system. Note that some of the interrupts are allocated dynamically.

	APIC C	ontroller	Interrupt Sig	nalling on
Interrupt Source	of device	Input	(PIC mode) ¹	(APIC modes)
INTA - PCI slot 3 (32/33)	P64H	IRQO	BT_INT	APIC bus
INTB - PCI slot 3 (32/33)	P64H	IRQ1	BT_INT	APIC bus
INTC - PCI slot 3 (32/33)	P64H	IRQ2	BT_INT	APIC bus
INTD - PCI slot 3 (32/33)	P64H	IRQ3	BT_INT	APIC bus
INTA - PCI slot 4 (32/33)	P64H	IRQ4	BT_INT	APIC bus
INTB - PCI slot 4 (32/33)	P64H	IRQ5	BT_INT	APIC bus
INTC - PCI slot 4 (32/33)	P64H	IRQ6	BT_INT	APIC bus
INTD - PCI slot 4 (32/33)	P64H	IRQ7	BT_INT	APIC bus
INTA - onboard SCSI controller	P64H	IRQ8	BT_INT	APIC bus
AGP - INTA, PCI Slot 1 - INTC, PCI Slot 2 - INTA, PCI Slot 5 - INTB	ICH2	INTA	INT	APIC bus
PCI Audio - INTA, AGP - INTB, PCI Slot 1 - INTD, PCI Slot 2 - INTB, PCI Slot 5 - INTC	ICH2	INTB	INT	APIC bus
BT_INT, PCI Slot 1 - INTA, PCI Slot 2 - INTC, PCI Slot 5 - INTD	ICH2	INTC	INT	APIC bus
USB - INTA, PCI Slot 1 - INTB, PCI Slot 2 - INTD, PCI Slot 5 - INTA	ICH2	INTD	INT	APIC bus
Device on Primary IDE Channel	ICH2	IRQ14	INT	APIC bus
Device on Secondary IDE Channel	ICH2	IRQ15	INT	APIC bus
Serial Interrupt from Super I/O	ICH2	SERIRO	INT	APIC bus

^{1.} In PIC mode, the Interrupts signaled to the P64H are chained as INTC to the ICH2.

There are three major interrupt modes available:

PIC mode: This mode uses only the "Legacy" interrupt controllers, so that only one processor can be supported. Because this system has dual processor capability, this mode is not chosen by default by Windows NT. However, during Windows NT installation, you have the possibility of selecting this mode.

Virtual wire mode: This mode is implemented with APIC controllers in the ICH2 and P64H and used during boot time. The virtual wire mode allows the transition to the "symmetric I/O mode". In the virtual wire mode, only one processor executes instructions.

Symmetric I/O mode: This mode is implemented with APIC controllers in the ICH2 and P64H, and allows for multiple processor operations.

NOTE

In "PIC mode" and "virtual wire mode", the PCI interrupts are routed to the INT line. In the "symmetric I/O mode", the PCI interrupts are routed to the I/O APIC controllers and forwarded over an APIC bus to the processors.

PCI Interrupt Request Lines

PCI devices generate interrupt requests using up to four PCI interrupt request lines (INTA#, INTB#, INTC#, and INTD#).

PCI interrupts can be shared; several devices can use the same interrupt. However, optimal system performance is reached when minimizing the sharing of interrupts. Refer to <u>page 59</u> for a table of the PCI device interrupts.

Assigned Device Interrupts

Interface Cards

This chapter describes the graphics, network and SCSI devices that are supplied with the *HP Kayak XU700 PC Workstation*.

Graphics Cards

HP Kayak XU700 PC Workstation models are supplied with a graphics card. This graphics card is one of the following, depending on the PC Workstation model:

- Matrox Millennium G450
- NVIDIA Quadro2 MXR.

Matrox Millennium G450 Graphics Card

The Matrox Millennium G450 Dual Head AGP graphics card has a total of 16MB of installed video memory (non-upgradeable). Main features include:

- Powered by the 256-bit DualBus Matrox G450 chip
- Matrox DualHead technology for connecting two monitors
- Matrox DualHead technology with PowerDesk desktop manager:
 - ☐ Easy multiple resolutions support
 - ☐ Simple dialog box
 - ☐ Effortless multiple-window management
- TV output (composite video and S-video, NTSC and PAL)
- Full AGP 2X/AGP 4X support (up to 1GB/s bandwidth)
- 360MHz main RAMDAC and 230MHz secondary RAMDAC
- Support for all VESA standards:
 - ☐ VBE 2.0 (Super VGA modes)
 - ☐ DPMS energy saving
 - ☐ DDC2B support for Plug & Play detection of monitor
- Support for true 32-bit color (16.7 million colors) at resolutions up to 2048 x 1536 on the main display.

3 Interface Cards

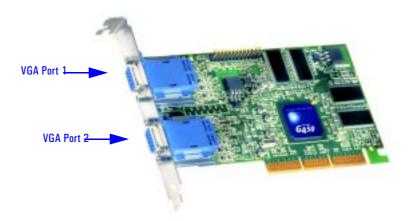
Graphics Cards

• Support for monitors with 16/10 aspect ration, at resolutions up to 1920×1200 on the main display

3D Features

- VCQ² or Vibrant Color Quality²
- Supports 32-bit Z buffering for exceptional rendering precision
- Environment-mapped bump mapping for more realistic 3D images.
- Stencil buffering
- Bilinear, trilinear, and anisotropic filtering
- Single, double and triple buffering
- texture mapping
- MIP mapping
- Gouraud shading
- Alpha blending, anti-aliasing, fogging, specular highlighting.

The diagram below shows the Matrox Millennium G450 graphics card.



NOTE

If only one monitor is used, then Port 1 must be used.

If a second monitor is connected, it is detected by the driver during the operating system startup. This means that both monitors must be connected to the graphics card *before* startup.

If only one monitor is detected, then only the mono head settings will be available in the Driver Configuration screens.

Available Video Resolutions

The number of colors supported is limited by the graphics device and the video memory. The resolution/color/refresh-rate combination is limited by a combination of the display driver, the graphics device, and the video memory. If the resolution/refresh-rate combination is set higher than the display can support, you risk damaging the display.

The following table summarizes the maximum supported resolutions.

Maximum Display Resolution						
Aspect Ratio	Main Display	Second Display				
Traditional 4:3 / 5:4 aspect ratio	2048 x 1536	1600 x 1200				
Wide screen 16:9 / 16:10 aspect ratio	1920 x 1200	1600 x 1024				

3 Interface Cards

Graphics Cards

The following table summarizes the maximum supported refresh rates.

The maximum refresh rates are always attainable with 8-bit or 16-bit color. They may not be attainable with 24-bit or 32-bit color *and* the highest refresh rates.

Maximum Refresh Rates (Hz)						
Aspect Ratio	Resolution	Main Display (360MHz RAMDAC)	Second Display (230MHz RAMDAC)			
	640x480	200	200			
	800x600	200	200			
	1024x768	160	160			
	1152x864	140	150			
Traditional 4:3 / 5:4 aspect ratio	1280x1024	120	120			
	1600x1200	100	85			
	1800x1440	85	_			
	1920x1440	85	_			
	2048x1536	85	_			
	856x480	200	200			
Wide screen	1280x720	160	140			
16:9 / 16:10 aspect ratio	1600x1024	120	90			
	1920x1080	110	_			
	1920x1200	100	_			

Limitations

- When using Windows 95 or Windows 98 in dual display mode, the graphics memory is equally between the two displays. In this case each display has 16 MB graphics memory.
- The second display supports only 16-bit and 32-bit color.
- 3D acceleration is only available when using 16-bit and 32-bit color.

NVIDIA Quadro2 MXR

The NVIDIA Quadro2 MXR graphics card has these main features:

- TwinView[™] architecture allows two simultaneous displays.
- Support for both DVI-I (digital LCD) and VGA (analog CRT) monitors
- AGP 4x with fast writes
- 350MHz RAMDAC
- Digital Vibrance Control (DVC) for accurate color adjustment giving bright, accurate colors in all conditions
- ?High performance hardware anti-aliasing for smoother edges

3D Features

- Second Generation Transform and Lighting Engines
 Dedicated, graphics-specific GPU frees PC Workstation's main processor for other tasks and provides faster transform and lighting processing.
- NVIDIA Shading Rasterizer
 Provides natural visual properties such as cloud, smoke, water, textiles,
 plastic to images.
- 32 MB Unified Frame Buffer Allows the use of high resolution, 32bpp textures.
- 32-bit Z/Stencil Buffer Eliminates "polygon popping" problems in high-polygon 3D imaging.

The diagram below shows an example of NVIDIA Quadro2 MXR graphics card.





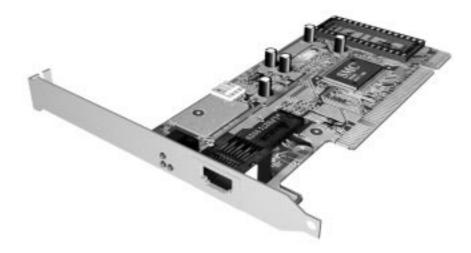
Network Cards

Most $HP\ Kayak\ XU700\ PC\ Workstation$ models are supplied with an HP 10/100 TX LAN card.

A description of this card and the features of other supported LAN cards is provided in this section.

HP 10/100 TX PCI LAN Interface

The 10/100 TX LAN Interface is a 32-bit PCI 2.2 card that supports 10 Mbits per second (10 BaseT) and 100 Mbits per second (100 TX) transfer speeds, and both half and full duplex operation.



HP 10/100 TX PCI LAN Interface Features

Feature:	Description:
RJ45 Connector	Connection to Ethernet 10/100 TX autonegotiation
BootROM	Protocols: • PxE 2.0, • On-board socket support up to 128 Kb.
Remote Power On (RPO)	Full remote power on using Magic Packet for Microsoft Windows 95, Windows NT4 in APM mode.
Remote Wake Up (RWU)	Enable and Wake Up from Suspend state using Magic Packet and Pattern Matching for Microsoft Win98SE and Win2000 in ACPI mode. This feature enables a host computer to remotely (over the network) power on computers and wake computers up from energy-saving Sleep mode. For these features to work, use the Setup program to configure the BIOS.
Power Management	 OnNow 1.0, Advanced Power Management 1.2, PCI Power Management 1.1, WfM 2.0 compliant, ACPI.
Manageability	 Desktop Management Interface (DMI) 2.0 Dynamic driver, DMI 2.0 SNMP mapper, PXE 2.0 Flashable BootROM (optional on socket).
Diagnostic	Mac address DOS report tool, User Diag for DOS.

HP 10/100 TX PCI LAN Interface LED Descriptions

LED	Description	Flashing	Steady	Off
10 LNK	Link integrity	Reversed polarity	Good 10 Base-T connection between NIC and hub.	No connection between NIC and hub
100 LNK	Link integrity	Reversed polarity	Good 100 TX connection between NIC and hub.	No connection between NIC and hub
ACT	Yellow: Port traffic for either speed	Network traffic present	Heavy network traffic	No traffic

3 Interface Cards

Network Cards

Supported LAN Cards

The following LAN cards are supported on the $HP\ Kayak\ XU700\ PC\ Workstation$.

$3 COM\ NIC\ (Network\ Interconnect)\ LAN\ Card$

3COM NIC LAN Card Features

Feature	Description
Interface	32-bit 10/100 BT full duplex RJ LAN Port.
LED	Three LEDs: activity,
	10 MB/s speed,100 MB/s speed.
Labels	PCI 2.2 Specification, PC 99, Intel WfM 2.0.
Power Management ¹	 RPO and RWU for APM Windows 95 and Windows 98, RWU for ACPI Windows 98 and Windows 2000, RPO for Windows NT 4, OnNow 1.0, APM 1.2, PCI power management. 1.1, WOL, PCI VccAux 3.3 V.
Manageability	DMI 2.0 Component Code.
Diagnostic	 Mac address DOS report tool, User Diag for DOS, Windows NT 4, Windows 95 and Windows 98.
Drivers	Major OSes, Minor OSes.
Boot ROM	Multiboot BootROM (BIOS or socket).
Remote Wake Up (RWU)	This feature enables a host computer to remotely (over the network) power on computers and wake computers up from energy-saving Sleep mode. For these features to work, use the Setup program to configure the BIOS.

3COM LAN Card LED Descriptions

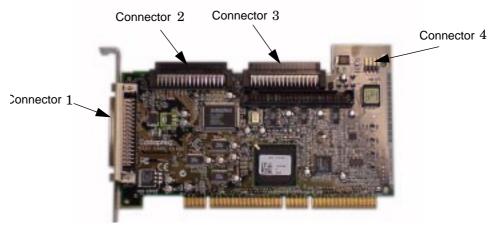
LED	Description	Flashing	Steady	Off
10 LNK	GREEN: Link integrity	Reversed polarity	Good 10 Base-T connection between NIC and hub.	No connection between NIC and hub
100 LNK	GREEN: Link integrity	Reversed polarity	Good 100 TX connection between NIC and hub.	No connection between NIC and hub
ACT	Yellow: Port traffic for either speed	Network traffic present	Heavy network traffic	No traffic

SCSI Adapter Cards

Adaptec 29160 SCSI PCI Adapter Card

Your Personal Workstation is equipped with an Ultra 160/m SCSI card. The Adaptec® SCSI card has a system bus rate of 533 MB/Sec, a SCSI data transfer rate of 160 MB/Sec and the capability of supporting up to 15 peripheral devices.

The Adaptec SCSI card is able to connect to Low-Voltage Differential (LVD) SCSI devices (for example, Ultra2 and Ultra 160/m) and Single-Ended (SE) SCSI devices (for example, Ultra SCSI, Fast SCSI, SCSI-1, etc.). Examples of single ended devices include: DAT drives, Scanners, and older hard disk drives.



Here is a description of connectors one through four.

Connector 1 68-pin external connector for LVD SCSI devices

Connector 2 68-pin internal connector for LVD SCSI devices

Connector 3 68-pin internal connector for Wide SE SCSI devices

Connector 4 50-pin internal connector for Narrow SE SCSI devices

While SE SCSI devices will work when attached to connector 1 or 2, this will limit all devices to single-ended mode. For example, this would result in the Ultra 160/m hard disk drive performance being limited from 160 MB/second to 40 MB/second. Therefore, it is recommended that you connect only LVD

SCSI devices to connectors 1 and 2.

For information on how to connect internal an external SCSI devices, please read your *User's Guide*.

SCSI Cable Information

The intended use of the external SCSI connector is to connect Low-Voltage Differential SCSI devices to your Personal Workstation. This section provides you with SCSI cable information that is important for the correct operation of your external SCSI device.

NOTE

The total length of the external SCSI cable should not exceed 10 meters (approximately 32.81 feet) and there must be at least eight inches of cable separating each device.

Contact you dealer to order shielded HP SCSI cables to connect external SCSI accessories.

CAUTION:

Low-voltage differential SCSI is very sensitive to noise, and therefore, all cables on the SCSI bus must be exceptionally high quality cables. Examples of these are given in the following table.

Please make sure that any external hard disk enclosures are rated for low-voltage differential SCSI use.

Cable Number	Cable Length	Description
C2978A	0.5m	68-pin HDTS ¹ to 68-pin HDTS
C2979A	1.5m	
C2911B	1.0m	
C2924B	2.5m	
C2361A	1.0m	68-pin VHDCI ² to 68-pin HDTS
C2362A	2.5m	
C2363A	10.0m	
C2365A	5.0m	

^{1.} High Density Thumbscrew (HDTS)

^{2.} Very High Density Cabled Interconnect (VHDCI)

3 Interface Cards

SCSI Adapter Cards

Additional SCSI Card Features

The Adaptec® SCSI card provides double transition clocking, cyclical redundancy check, and domain validation.

Feature	Description
Double Transition Clocking	Changes the digital protocol to use both edges of the SCSI request/acknowledge signal clock. It allows designers to use Ultra2 cables. The signal in an Ultra2 SCSI runs a 40 MHz, while data runs at only 20 MHz or 80 MB/second on a 16-bit wide bus.
	Using both edges of the same signal at 40 MHz the data rate can be increased to 40 MB/second or 160 MB/second on a 16-bit wide bus.
Cyclical Redundancy Check	Provides extra data protection for marginal cables that are connected to external devices. The Ultra3 SCSI cyclical redundancy check detects all:
	 Single error bits Double bit errors Odd number of errors Burst errors up to 32-bits long
Domain Validation	Tests networks, cables, backplanes, terminators, and hard disk drives to ensure that the environment is operating at required specification. If reliability is at risk the speed of transfer is lowered.

Mass Storage Devices

This chapter describes the mass storage devices that are supplied with the PC Workstation. For the position of the different mass storage devices, refer to the diagram on <u>page 13</u>. This chapter also summarizes the pin connections on internal and external connectors.

HP product numbers and replacement part numbers for mass storage devices are listed in the Service Handbook Chapters, which can be accessed from the HP World Wide Web site at the following address:

www.hp.com/go/kayaksupport.

Information about available accessories can be obtained from www.hp.com/go/pcaccessories

Flexible Disk Drives

A 3.5-inch, 1.44 MB flexible disk drive is supplied in the front-access shelf.

Hard Disk Drives

The following table lists the 3.5-inch (1-inch high) hard disk drives (which are subject to change) that may be supplied with the *HP Kayak XU700 PC Workstation* (type and quantity depends on model) on internal shelves, connected to the SCSI or IDE controller.

IDE Hard Disk Drives

	IBM Deskstar 75GXP IDE (7.2 krpm)	IBM Deskstar (Telesto LP) 75GXP IDE (7.2 krpm)
Capacity	20.5 GB	40 GB
Interface	UltraIDE ATA/66	UltraIDE ATA/66
External peak transfer rate	66 MB/s	66 MB/s
Average seek time (read)	8.5 ms	8.5 ms
Media transfer rate (Mb/s)	444 Mb/s max.	444 Mb/s max.
Number of discs/heads	2/3	3/6
Buffer size	2 MB	2 MB

4 Mass Storage Devices

SCSI Hard Disk Drives

	Quantum Atlas 10K II SCSI (10 krpm)	Quantum Atlas 10K II SCSI (10 krpm)	Quantum Atlas 10K II SCSI (10 krpm)
Capacity	9.2 GB	18.4 GB	36.7 GB
Interface	Ultra160 SCSI	Ultra160 SCSI	Ultra160 SCSI
External peak transfer rate	160 MB/s	160 MB/s	160 MB/s
Average seek time (read)	4.7 ms	4.7 ms	4.7 ms
Internal data rate (Mb/s)	280 Mb/s min. to 478 Mb/s max.	280 Mb/s min. to 478 Mb/s max.	280 Mb/s min. to 478 Mb/s max.
Number of discs/heads	2/3	3/6	5/10
Buffer size	8 MB	8 MB	8 MB

CD-ROM Drives

IDE 48X CD-ROM Drive

Some models¹ have a 48X IDE CD-ROM drive supplied in a 5.25-inch front-access shelf ATAPI, supporting ATAPI commands and with audio playback capability. It can play any standard CD-Audio disks, in addition to CD-ROM disks, conforming to optical and mechanical standards as specified in the Red, Yellow, Green and Orange Book.

Some of the 48X IDE CD-ROM features include:

- Application Disk type (confirmed by Red, Yellow, Green, Orange Book)
- CD-ROM data disk (Mode 1 and Mode 2)
- Photo-CD Multisession
- CD Audio disk
- Mixed mode CD-ROM disk (data and audio)
- CD-ROM XA, CD-I, CD-Extra, CD-R, CD-RW

	Description
Data capacity	650 MB
Data transfer rate	Sustained transfer rate (1X = 150 KB/s); Outerside: 7,200 KB/s
	Burst transfer rate:
	PIO mode 4 - 16.6 Mbytes/s maximum
	Single Word DMA Mode 2 - 8.3 Mbytes/s maximum
	Multi Word DMA Mode 2 - 16.6 Mbytes/s maximum
Buffer memory size	128 Kbytes
Access time	Average Stroke (1 / 3) 110 ms
	Full Stroke 180 ms
Rotational speed	2,048 bytes (Mode-1)
	2,336 bytes (Mode-2)
Interface	ATAPI
Power requirements	5V, 1.2A
	12V, 0.8A

^{1.} Refer to the HP Kayak PC Workstations Service Handbook to find out which models are installed with the 48X IDE CD-ROM.

4 Mass Storage Devices

8X Video IDE DVD-ROM Drive

Some models¹ have a DVD-ROM (Read Only) drive. It can play any standard CD-Audio disks, in addition to CD-ROM disks, conforming to optical and mechanical standards as specified in the Red, Yellow, Orange and Green Books.

	Description
Data capacity	650 MB
Data transfer rate	Sustained transfer rate (1X = 150 KB/s); Outerside: 7,200 KB/s
	Burst transfer rate:
	PIO mode 4 - 16.6 Mbytes/s maximum Single Word DMA Mode 2 - 8.3 Mbytes/s maximum Multi Word DMA Mode 2 - 16.6 Mbytes/s maximum
Buffer memory size	128 Kbytes
Access time	Average Stroke (1 / 3) 110 ms
	Full Stroke 180 ms
Rotational speed	2,048 bytes (Mode-1)
	2,336 bytes (Mode-2)
Interface	ATAPI
Power requirements	5V, 1.2A
	12V, 0.8A

^{1.} Refer to the HP Kayak PC Workstations Service Handbook to find out which models are installed with the DVD-ROM drive.

4X IDE CD-Writer Plus Drive

Some models¹ have a CD-RW (ReWritable) drive supplied in a 5.25-inch front-access shelf ATAPI, supporting ATAPI commands and with audio playback capability. It can play any standard CD-Audio disks, in addition to CD-ROM disks, and can record both write-once (CD-R) and CD-RW optical media. It conforms to optical and mechanical standards as specified in the Red, Yellow, Orange and Green Books.

	Description
Data capacity	650 MB or up to 74 minutes of audio per disc
	547MB in CD-UDF data format
Performance	Typical: 110 ms (random, 1/3 access including latency)
	Maximum: 130 ms (random, 1/3 access including latency)
	Data transfer rate: Read: Up to 32X (1X = 150 KB/s) Write: 8X (CD-R); 4X (CD-RW)
Burst transfer rate	16.67 Mbytes/sec.
Spin-up time	3.2 seconds (disk stop to high speed)
Spin-down time	2.5 seconds (disk high speed to stop)
Corrected error rate	ECC On (max. 32X): 1 block/10 ¹² bits
	ECC Off (max. 32X): 1 block/10 ⁹ bits
Data Buffer Capacity	2 MB
Write methods	- Track at once - Session at once - Disc at once - Variable packet writing
	- Fixed packet writing - Multisession
Format and EEC standard	Red, Yellow, Orange, Green books
MTBF	120,000 POH
Interface	E-IDE and ATAPI

^{1.} Refer to the HP Kayak PC Workstations Service Handbook to find out which models are installed with the HP CD-RW drive.

4 Mass Storage Devices

HP BIOS

This chapter summarizes the *Setup* program and BIOS of the *HP Kayak XU700 PC Workstation*. The POST routines are described in the next chapter.

The BIOS is based on the core Phoenix BIOS, which includes 4 M/bits of flash memory, support for PCI 2.2 Specification, suspend to RAM, and RIMM or DIMM memory modules.

The BIOS includes a Boot ROM for the 3COM 3C905C and HP LAN cards.

The System ROM contains the POST (Power-On Self-Test) routines, and the BIOS: the System BIOS, video BIOS, and low option ROM. This chapter, together with the subsequent chapter, gives an overview of the following aspects:

- Menu-driven *Setup* with context-sensitive help, described next in this chapter.
- The address space, with details of the interrupts used, described at the end of this chapter.
- The Power-On Self-Test or POST, which is the sequence of tests the computer performs to ensure that the system is functioning correctly, described in the next chapter.

The system BIOS is identified by the version number IX. WM, where:

- *IX* is a two-letter code indicating that it is for the Kayak XU700.
- W is a one-digit code indicating the HP entity.
- *M* is the major BIOS version.

An example of a released version would look similar to the following the example: IX.W1.05.

The procedure for updating the System ROM firmware is described on page 87.

Using the HP Setup Program

To run the *Setup* program, press **F2** while the initial HP logo is displayed, immediately after restarting the PC Workstation.

Alternatively, press (Esc.) to view the summary configuration screen. By default, this remains on the screen for 15 seconds, but pressing any key will ignore this delay.

The band along the top of the *Setup* screen offers the following menus: Main, Advanced, Security, Boot, Power and Exit. These are selected using the left and right arrow keys.

The following screens are examples of a BIOS configuration.

Main Screen

The Main Screen presents a list of fields. To change a value press either the F7 or F8 keys.

	PhoenixBIOS Setup Utility								
N	lain		Advanced	Securi	ity	Boot	Power	Exit	
								Item-Sp	ecific Help
	BIOS Vers	sion:		IC.11.02					
	PnP OS Reset Cor	nfiguration	ı Data:	[No] [No]					
	System T System D			[14:42:33] [02/08/2000]					
	Key Click: Keyboard Delay bef Numlock	auto-repe ore auto-r		[Disabled] [21.8 per Seco [0.50 Second] [On]	nd]				
F1	Help	1	Ψ	Select Item	F7/F8	Change	Values	F9	Setup Defaults
ESC	Exit	←	→	Select Menu	Enter	Select >	Sub-Menu	F10	Previous Values

Advanced Screen

The Advanced Screen does not have the same structure as the Main Screen and Power Screen. Instead of presenting a list of fields, it offers a list of sub-menus.

The Advanced screen is to be used by advanced users who wish to carry out special system configurations.

Main	Advanced	Security	Boot	Power	Exit
					Item-Specific Help
>> Processors	, Memory and Cache				
>> Floppy Disl	C Drives				
>> IDE Device	S				
>> Integrated	USB Interface				
>> Integrated	I/O Ports				
>> Integrated	Audio Device				
>> AGP Confid	guration (Video)				
>> PCI Device	, slot #1				
>> PCI Device					
>> PCI Device	. slot #3				
>> PCI Device					
>> PCI Device					

Processors, Memory and Cache

Advanced	Advanced	
Processor	s, Memory and Cache	Item-Specific Help
Processor Type CPU Speed	Pentium (R) 4 1500 MHz	
Processor Serial Number	[Disabled]	
Memory Caching Memory Error Checking ¹	[Enabled] [Disabled]	

Only if ECC modules are detected.

Floppy Disk Drives

Advanced		
Floppy Disk Drives		Item-Specific Help
Floppy Disk Controller	[Enabled]	
Floppy Disk Drive A Floppy Disk Drive B	[1.44, 3½"] [Not installed]	

IDE Devices

Advanced		
IDE Devices		Item-Specific Help
>> IDE Primary Master Device >> IDE Primary Slave Device	[None] [None]	
>> IDE Secondary Master Device >> IDE Secondary Slave Device	[None] [None]	
>> Large Disk Access Method >> Integrated IDE Controller	[NT/DOS] [Both Enabled]	

IDE Primary Master Device

Advanced		
IDE Primary Master Device (HD 2564)	Item-Specific Help	
Туре		
Multisector transfer		
LBA Mode Control		
32 bit I/O		
Transfer Mode		
ULTRA DMA Mode		
OLITIA DINIA INIOUE		

Integrated USB Interface

Advanced		
Integrated	USB Interface	Item-Specific Help
USB Controller	[Auto]	
Legacy Keyboard Emulation	[Disabled]	

Integrated I/O Ports

Advanced		
Integrat	Integrated I/O Ports	
Parallel Port Parallel Port Mode Serial Port A Serial Port B	[Auto] [ECP] [Auto] [Auto]	

Integrated Audio Device

Advanced		
Integrated Audio Device		Item-Specific Help
Integrated Audio	[Enabled]	

AGP Configuration (Video)

	Advanced	
AGP Configuration (Video)		Item-Specific Help
Graphic Aperture	[64 MB]	

PCI Device, Slot #1

Advand	ed	
PCI De	vice, Slot 1 ¹	Item-Specific Help
Option ROM Scan	[Auto]	
Bus Master Bus Latency Timer	[Disabled] [0040h]	

^{1.} PCI Slot #x have the same options as above. PCI Device, Slot 1 is only used as an example.

Security Screen

Sub-menus are presented for changing the characteristics and values of the System Administrator Password, User Password, Power-on Password, boot device security and Hardware Protection.

Vlain Adv	anced	Security	Boot	Power	Exit
					Item-Specific Help
Administrator Password Set Administrator Passw Clear Both Passwords	Clear rord [Enter] [Enter]				
User Password Set User Password	Clear [Enter]				
Power-on Password	[Disable	ed]			
Start from Floppy Start from CD-ROM Start from HDD	[Enable [Enable [Enable	d]			
Hardware Protection					

Hardware Protection

	Security	
Hardware P	rotection	Item-Specific Help
Write on Floppy Disks	[Unlocked]	
ecured Setup Configuration ard Disk Boot Sector	[No] [Unlocked]	

Boot Screen

This screen allows you to select the order of the devices in which you want the BIOS to attempt to boot the operating system:

- Hard disk drives
- Removable devices.

The operating system assigns drive letters to these devices in the order you specify. During POST, if the BIOS is unsuccessful at booting from one device, it will then attempt to boot from the next device on the *Boot Device Priority* list until an operating system is found.

Main	Advanced	Security	Boot	Power	Exit
					Item-Specific Help
Quickboot M Display Opti	Mode on ROM Messages	[Enabled] [Enabled]			
> Boot Device	Priority				

Power Screen

This screen allows you to set the standby delay and suspend delay. Standby mode slows down the processor, while the suspend mode saves a maximum of energy. Both these options are only available with Windows 95 RTM. For other operating systems, Windows 95 SR 2.5, Windows 98 and Windows 2000, use the control panel for similar options.

Modem ring enables or disables the system to return to full speed when an IRQ is generated. Network interface enables or disables the system to return to full speed when a specific command is received by the network interface.

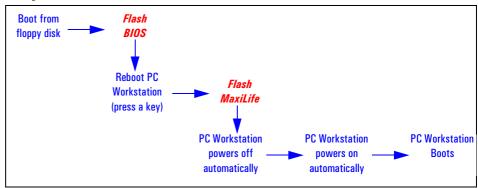
Main	Advanced	Security	Boot	Power	Exit
					Item-Specific Help
Standby Dela Suspend Dela		[Disabled] [Disabled]			
Suspend Wak Modem Ring Network Inte		[Enabled] [Enabled]			

Updating the System BIOS

The latest system BIOS (standard flash operation) can be downloaded from HP's Support Web site at: www.hp.com/go/kayaksupport. Then select HP Kayak XU700 PC Workstation.

Instructions on updating the BIOS are supplied with the downloaded BIOS files and a BIOS flash utility (flash.txt).

The BIOS update not only flashes the BIOS, but also updates MaxiLife. How the System BIOS flash is carried out is shown below.



Do not switch off the computer until the system BIOS update procedure has completed, successfully or not, otherwise irrecoverable damage to the ROM may be caused.

Restoring BIOS Default Settings

Suspected hardware errors may be caused by BIOS and configuration issues. If the BIOS settings are suspected to be wrong, do the following steps to restore the BIOS to its default setting:

- 1 Press [2] while the initial HP logo is displayed immediately after restarting the PC Workstation to access the *Setup* program.
- 2 Press (5) to load the default settings from the *Setup* program.
- 3 Set the "Reset Configuration Data" to Yes in the Main menu. It is recommended that before you make any modifications to the BIOS you take note of the system setup.

If You Forgot the Administrator Password

- 1 Switch off the PC Workstation and remove the power cord.
- 2 Remove the PC Workstation's cover.
- 3 Set switch 9 on the system board switch block to the ON position.
- 4 Replace the power cord and restart the PC Workstation.
- 5 When the message *Passwords have been cleared* appears on screen, switch off the PC Workstation.
- 6 Remove the power cord and reset switch 9 back to the OFF position.
- 7 Replace the PC Workstation's cover.
- 8 Switch on the PC Workstation and allow it to complete its startup routine.
- 9 After the Power-On-Self-Test has completed, press ${\bf F2}$ when prompted to use the Setup program.
- 10 Set the Administrator and new User passwords.
- 11 Press **Esc** or select **Exit Menu** to save the new Password and exit *Setup*.

Clearing the CMOS

- 1 Turn off the PC Workstation, disconnect the power cord and all cables, then remove the cover.
- 2 Set the system board switch 8 to the ON position.
- 3 Replace the cover, and reconnect the power cord and video cable.
- 4 Reboot the PC Workstation. A message similar to the following will be displayed:

"Configuration has been cleared, set switch Clear to the ON position before rebooting."

- 5 Turn off the PC Workstation, disconnect the power cord and video cable, and remove the cover.
- 6 Set the system board switch 8 to the OFF position.
- 7 Replace the cover, and reconnect the power cord and data cables.
- 8 Switch on the PC Workstation. Run the *Setup* program by pressing **F2**. Then press **F9**, the CMOS default values will be automatically downloaded and saved.
- 9 Press **Esc** to save the configuration and exit from the *Setup* program.

Recovering the BIOS (Crisis Mode)

If for some reason the BIOS is corrupted and the standard flash cannot be used, use the BIOS Recovery Mode (exceptional BIOS recovery operation) to restore the BIOS. To do this:

- 1 Obtain a bootable DOS floppy disk.
- 2 Copy the BIOS files on to the floppy disk. How to download the system BIOS is described on page 87.
- 3 Create (or edit) the file, AUTOEXEC.BAT
 This should contain a single line of text:
 "phlash /c /mode=3 /s IX.W1.XX.FUL"
 (rename the BIOS filename with the one on the floppy disk).
- 4 Shut down the PC Workstation.
- 5 Power off the PC Workstation and remove the power cord.
- 6 Remove the cover.
- 7 Set switch 7 to the ON position.
- 8 Insert the floppy disk into the floppy disk drive.
- 9 Reconnect the power cord and switch on the PC Workstation.
- 10 The PC Workstation boots from the floppy disk, then flashes the BIOS. However, it should be noted, that during the flash process, the screen remains blank.
- 11 The recovery process is finished when there is one very long beep.
- 12 Power off the PC Workstation. Remove the floppy disk from the drive. Remove the power cord.
- 13 Set switch 7 back to the OFF position.
- 14 Replace the cover, reconnect the power cord, then reboot the PC Workstation.

BIOS Addresses

This section provides a summary of the main features of the HP system BIOS. This is software that provides an interface between the computer hardware and the operating system. The procedure for updating the System ROM firmware is described on page 87.

System Memory Map

Reserved memory used by accessory boards must be located in the area from C8000h to EFFFFh.

0000 0000 - 0000 03FF	Real-mode IDT
0000 0400 - 0000 04FF	BIOS Data Area
0000 0500 - 0009 FC00	Used by Operating System
0009 FC00 - 0009 FFFF	Extended BIOS Data Area
000A_0000 - 000B_FFFF	Video RAM or SMRAM (not visible unless in SMM)
000C 0000 - 000C 7FFF	Video ROM (VGA ROM)
000C 8000 - 000F FFFF	Adapter ROM, RAM, memory-mapped registers, BIOS
000E 0000-000F FFFF	128 KB BIOS (Flash/Shadow)
0001 0000-000F FFFF	Memory (1 MB to 16 MB)
0010 0000-001F FFFF	Memory (16 MB to 32 MB)
0020 0000-003F FFFF	Memory (32 MB to 64 MB)
0040 0000-007F FFFF	Memory (64 MB to 128 MB)
0080 0000-7FFF FFFF	Memory (128 MB to 2 GB)
FECO 0000	I/O APIC
FEE0 0000	Local APIC (each CPU)
FFF8 0000-FFFF FFFF	512 KB BIOS (Flash)

HP I/O Port Map (I/O Addresses Used by the System¹)

Peripheral devices, accessory devices and system controllers are accessed via the system I/O space, which is not located in system memory space. The 64 KB of addressable I/O space comprises 8-bit and 16-bit registers (called I/O ports) located in the various system components. When installing an accessory board, ensure that the I/O address space selected is in the free area of the space reserved for accessory boards (100h to 3FFh).

Default Values for I/O Address Ports	Function
0000 - 0CF7	DMA controller 1
0020 - 0021	Master interrupt controller (8259)
002E - 002F	Super I/O
0040 - 0043	Timer 1
0060, 0064	Keyboard controller (reset, slow A20)
0061	Port B (speaker, NMI status and control)
0070	Bit 7: NMI mask register
0070 - 0071	RTC and CMOS
0080	Manufacturing port (POST card)
0081 - 0083, 008F	DMA low page register
0092	PS/2 reset and Fast A20
00A0 - 00A1	Slave interrupt controller
00CO - 00DF	DMA controller 2
00F0 - 00FF	Co-processor error
0170 - 0177	Free (IDE secondary channel)
01F0 - 01F7	IDE primary channel
0278 - 027F	LPT 2
02E8 - 02EF	Serial port 4 (COM4)
02F8 - 02FF	Serial port 2 (COM2)
0372 - 0377	Free (IDE secondary channel, secondary floppy disk drive)
0378 - 037F	LPT1
03B0 - 03DF	VGA
03E8 - 03EF	COM3
03F0 - 03F5	Floppy disk drive controller
03F6	IDE primary channel
03F7	Floppy disk drive controller

1.If configured.

Default Values for I/O Address Ports	Function
03F8 - 03FF	COM1
04D0 - 04D1	Interrupt edge/level control
0778 - 077F	LPT1 ECP
OCF8 - OCFF	PCI configuration space
C000 -	Power Management I/O space and ACPI Registers
C100 - C10F	SMBus I/O space

DMA Channel Controllers

Only "I/O-to-memory" and "memory-to-I/O" transfers are allowed. "I/O-to-I/O" and "memory-to-memory" transfers are disallowed by the hardware configuration.

The system controller supports seven DMA channels, each with a page register used to extend the addressing range of the channel to 16 MB.

The following table summarizes how the DMA channels are allocated.

DMA controller			
Channel	Function		
DMA 0	Free		
DMA 1	Free if not used for parallel port in <i>Setup</i>		
DMA 2	Floppy disk drive controller		
DMA 3	Free if not used for parallel port in <i>Setup</i>		
DMA 4	Used to cascade DMA channels 0-3		
DMA 5	Free		
DMA 6	Free		
DMA 7	Free		

Interrupt Controllers

The system has an Interrupt controller which is equivalent in function to that of two 82C59 interrupt controllers. The following table shows how the interrupts are connected to the APIC controller. The Interrupt Requests (IRQ) are numbered sequentially, starting with the master controller, and followed by the slave (both of 82C59 type).

I/O APIC Input	IRQ	Interrupt Request Description
INTINO	ICH	
INTIN1	IRQ1	Super I/O Keyboard Controller
INTIN2	IRQ0	ICH System Timer
INTIN3	IRQ3	Super I/O - Used by serial port if enabled
INTIN4	IRQ4	Super I/O - Used by serial port if enabled
INTIN5	IRQ5	Free if not used for parallel port or audio
INTIN6	IRQ6	Super I/O - Floppy Disk Controller
INTIN7	IRQ7	Super I/O - LPT1
INTIN8	IRQ8	ICH - RTC
INTIN9	IRQ9	Available for PCI devices
INTIN10	IRQ10	Available for PCI devices
INTIN11	IRQ11	Available for PCI devices
INTIN12	IRQ12	Super I/O - Mouse
INTIN13	IRQ13	Co-processor
INTIN14	IRQ14	ICH - Integrated IDE Controller (primary)
INTIN15	IRQ15	ICH - Integrated IDE Controller (secondary).
INTIN16	PCINTA	
INTIN17	PCINTB	
INTIN18	PCINTC	
INTIN19	PCINTD	
INTIN20	TFPC IRQ	
INTIN21	SCI IRQ	
INTIN22	not connected	
INTIN23	ICH SMI (not used)	

There are three major interrupt modes available:

PIC mode: This "Legacy" mode uses only the interrupt controllers. Therefore, only one processor can be supported in this mode. This mode can be selected upon installation of Windows NT.

Virtual wire mode: This mode is implemented using the 82C59 interrupt and the I/O APIC controller and is used during boot time. The virtual wire mode allows the transition to the "symmetric I/O mode". In the virtual wire mode, only one processor executes operations.

Symmetric I/O mode: This mode is implemented using the I/O APIC controller and allows for multiple processor operations.

NOTE

In "PIC mode" and "virtual wire mode", the PCI interrupts are routed to the INT line. In the "symmetric I/O mode", the PCI interrupts are routed to the I/O APIC controllers and forwarded over an APIC bus to the processors.

PCI Interrupt Request Lines

PCI devices generate interrupt requests using up to four PCI interrupt request lines (INTA#, INTB#, INTC#, and INTD#).

PCI interrupts can be shared; several devices can use the same interrupt. However, optimal system performance is reached when minimizing the sharing of interrupts. Refer to <u>page 59</u> for a table of the PCI device interrupts.

5 HP BIOS

BIOS Addresses

Tests and Error Messages

This chapter describes the MaxiLife firmware test sequences and error messages, the pre-boot diagnostics error codes, the Power-On Self-Test (POST) routines, which are contained in the computer's ROM BIOS, the error messages which can result, and the suggestions for corrective action.

MaxiLife Test Sequence and Error Messages

When the PC Workstation is turned on (pressing the ON/OFF button), the system initiates the normal startup sequence which is composed of the following steps:

- Basic pre-boot diagnostics
- BIOS launch
- POST phase
- Operating System boot phase

If any errors are detected during the startup sequence, MaxiLife will not necessarily 'freeze' the system. However, some critical hardware errors are fatal to the system and will prevent the system from starting (for example, 'CPU Socket' and 'Power Supply' are serious malfunctions that will prevent the system from working correctly).

Errors that are not so critical will be detected both during pre-boot diagnostics and POST where the BIOS boot process will return an error code. Some errors are only detected during POST sequence, and produce the same process.

Finally, while the PC Workstation is working, fan and temperature controls can be reported (for example, a fan error will be reported if a fan cable is not connected). This type of error disappears as soon as the problem is fixed (for example, the fan cable has been reconnected).

The different diagnostics are described below.

6 Tests and Error Messages

MaxiLife Test Sequence and Error Messages

Basic Pre-boot Diagnostics

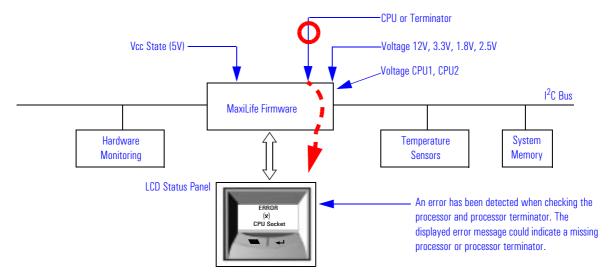
The first diagnostic (called basic pre-boot diagnostics) is run to check the presence of the processor(s) or terminators, power supply, hardware monitoring and thermal sensors. Simply by having a power cord connected to the PC Workstation activates the Basic Pre-boot Diagnostics.

The pre-boot diagnostic tests are run in order of priority with respect to their importance to computer functions.

On the *HP Kayak XU700 PC Workstation*, the first detected error displays a message on the LCD status panel. If this happens, one of the following screens could appear.



The following diagram shows how the Pre-boot Diagnostics works when it encounters an error.



The following table shows the test sequence carried out, the type of error message, and the action to take.

Test	Error Code	Beep Codes	Action to Take
Presence of either a processor or processor terminator	CPU Socket	1	Check that the processor(s), processor terminator are correctly installed.
Control of some voltages: 12V, 3.3V, 1.8V, 2.5V	Power Supply	2	Check the power supply cable and connectors, and processor.
Check the hardware monitoring.	No HW Monitoring		System board problem.
Check thermal sensor.	Therm. Sensor 90		System board problem.
Check thermal sensor.	Therm. Sensor 92		System board problem.

Pre-boot Diagnostics Error Codes

When a failure occurs prior to operating system loading, the PC emits a distinctive modulated sound (repeated three times), followed by a series of beeps. These beeps identify the part that needs troubleshooting or replacement.

Number of beeps	Problem
1	Absent or incorrectly connected processor.
2	Power supply is in protected mode.
3	Memory modules not present, incompatible or not functioning.
4	Video controller failure.
5	PnP/PCI initialization failure.
6	Corrupted BIOS. You need to activate crisis recovery procedure.
7	System board failure.

6 Tests and Error Messages

MaxiLife Test Sequence and Error Messages

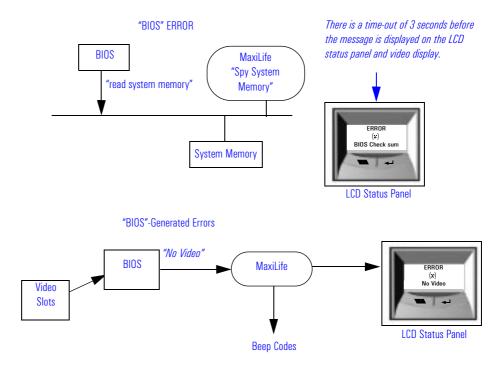
Post Test Sequence and Post Error

In this phase, MaxiLife waits for any error messages that the BIOS may issue. If such an error occurs, then an error code is displayed on the monitor screen.

On the *HP Kayak XU700 Minitower PC Workstation*, a screen similar to the following example is displayed. The error code that appears on the LCD status panel is the same as the one that appears on the monitor screen. If the POST issues several error codes, only the last one is visible on the LCD status panel.



The following diagrams show the different BIOS-generated errors.



Test	Error Code	Beep Codes	Action to Take	
Incompatible memory modules	Mem Miscompare	3	Check that the memory modules are of the same speed and type.	
Presence of continuity modules in the RIMM sockets	RIMM Continuity	3	Check that the RDRAM continuity modules are installed	
Compatibility speed rating of installed RDRAM modules	RIMM speed	3	Check that the installed RDRAM modules have the same speed ratings	
Compatibility of installed RDRAM modules	RIMM Devices	3	The 32 device limit per RDRAM has been exceeded.	
Presence of memory modules	No RIMM	3	Check that the memory modules are correctly installed	
Availability of video controller. It is checked by the BIOS. If an error is detected, it is not a fatal	No Video	4	Check that the video controller is correctly installed	
one and the BIOS will continue its execution normally.			Note: No error is detected if a monitor is not connected to an installed video controller. This is not a fatal error and the BIOS will continue its normal execution.	

Operating System Boot Phase

If no error message has been displayed at this stage of the system startup by the BIOS, the operating system is launched. The LCD status panel will display the system platform and a "smiling icon."

Run-Time Errors

During the normal usage of the PC Workstation (and at boot), MaxiLife continually monitors vital system parameters. These include: temperature errors, fan malfunctions, power voltage drops and CPU problems.

6 Tests and Error Messages

MaxiLife Test Sequence and Error Messages

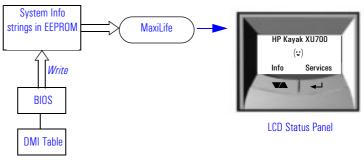
Test	Error Code	Action to Take
During normal usage of the PC, HP MaxiLife	System FAN	System or chassis fan, fan cable.
continually checks vital system parameters. If an error occurs, a message appears on the LCD	PCI FAN	PCI fan, fan cable.
panel.	CPU 1 FAN	CPU 1 fan, fan cable.
	CPU 2 FAN	CPU 2 fan, fan cable.
	Processor Temp	Processor temperature > 85°C.
	CPU Temperature	Thermal or internal processor failure.
	PCI Temperature	Ambient or PCI temperature > 64°C.
	Disk Temperature	Disk temperature > 58°C, or sensor unplugged.
	PSU 12 V error	Power supply unit has failed. Try the following:
	Power CPU error	1 Replace the power supply unit with a known working one.
	PSU 3V3 error	2 If the problem persists, replace the system board.
	PSU 2V5 error	
	PSU 1V8 error	
	PSU -5V error	

Main Menu (Minitower models only)

The main menu is displayed when any of the LCD buttons are pressed (MaxiLife LCD status panel can be accessed even though the PC Workstation is turned off). The Main Menu comprises three sub-menus: System Info, Boot Steps and Boot report.

System Info

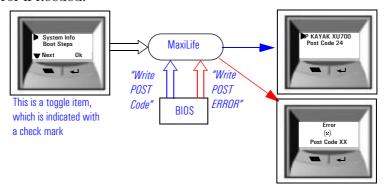
Obtains information from the BIOS and the system's Serial EEPROM. This information includes: product name, BIOS version, serial number, number of processors and speed, size of memory for each socket. The following diagram shows how the System Info obtains its information.



Boot Steps

Shows the Power-On-Self-Test (POST) codes during the system startup. The POST code is provided by the BIOS and is displayed on the LCD panel as soon as it is available. If the system stops during the startup, the last successful boot step POST code is displayed on the LCD. When Boot Steps is selected, the POST step will be shown on the LCD status panel during the subsequent boot processes.

To ensure that MaxiLife is ready to display the first POST codes as soon as possible, the Pre-boot diagnostics are not executed when the system is booted with the Boot Steps option selected. The following diagram shows how Boot Steps obtains its information from the BIOS, and then displays a POST error if needed.



Boot report

Runs a set of diagnostics assessing the system's components. Results of the tests are displayed on the LCD status panel, one after another, when the LCD \blacktriangleright buttons are pressed.

6 Tests and Error Messages

MaxiLife Test Sequence and Error Messages

Components are tested in sequence when the "Next" button is pressed. When they have all been checked, a diagnostic screen is shown. Depending on the result of the diagnostics, the screen could indicate either: Diagnostics Done OK or FAIL.

At the end of the test, you can exit the diagnostic mode by pressing the $\buildrel\square$ LCD button.

For More Information About MaxiLife

Refer to the online *Troubleshooting Guide* for more information about this diagnostics utility at the HP World Wide Web site:

http://www.hp.com/go/kayaksupport.

Order in Which POST Tests Are Performed

Each time the system is powered on, or a reset is performed, the POST is executed. The POST process verifies the basic functionality of the system components and initializes certain system parameters.

The POST starts by displaying a graphic screen of the HP PC Workstation's logo when the PC Workstation is restarted. If you wish to view the POST details, press **Esc** to get the HP Summary Screen.

If the POST detects an error, the screen switches to text mode, and a detailed error message is displayed inside a view system errors screen, in which the error message utility (EMU) not only displays the error diagnosis, but the suggestions for corrective action (refer to page 113 for a brief summary).

On the HP Kayak XU700 Minitower PC Workstation, the LCD status panel displays either a message, a POST code number (refer to page 105) or an EMU code.

Devices such as memory and newly installed hard disks, are configured automatically. The user is not requested to confirm the change.

During the POST, the BIOS and other ROM data are copied into high-speed shadow RAM. The shadow RAM is addressed at the same physical location as the original ROM in a manner which is completely transparent to applications. It therefore appears to behave as very fast ROM. This technique provides faster access to the system BIOS firmware.

The following table lists the POST checkpoint codes and their associated beeps. Refer to page 99 for more details about pre-boot diagnostics error codes.

Checkpoint Code	POST Routine Description	MaxiLife LCD Display Message	Beep Codes
02h	Verify Real Mode		
03h	Disable Non-Maskable Interrupt (NMI)		
04h	Get CPU type		

06h Initialize system hardware 08h Initialize chipset with initial POST values 09h Set IN POST flag P.O.S.T Start 0Ah Initialize CPU registers CPU Regist. Init 0Bh Enable CPU cache CPU Regist. Init 0Ch Initialize caches to initial POST values I/O Init. 0Eh Initialize I/O component I/O Init. 0Fh Initialize House IDE IDE Init. 10h Initialize Power Management Initialize Power Management 11h Load alternate registers with initial POST values 12h Restore CPU control word during warm boot 13h Initialize PCI Bus Mastering devices PCI Mast. Init. 14h Initialize keyboard controller 16h BIOS ROM checksum BIOS Check sum 17h Initialize cache before memory autosize BIOS Check sum 17h Initialize cache before memory autosize Initialize Cache before memory autosize 18h 8254 timer initialization Initialize Cache before memory autosize 12h Test DRAM refresh RAM Refresh Test 22h Test BRAV2 keyboard controller Keyb. Ctrl. Test 24h Set ES segment register to 4 GB Keyb. Ctrl. Test 28h Autosize DRAM <	Checkpoint Code	POST Routine Description	MaxiLife LCD Display Message	Beep Codes
O9h Set IN POST flag P.O.S.T Start OAh Initialize CPU registers CPU Regist. Init OBh Enable CPU cache OCh Initialize caches to initial POST values OEh Initialize I/O component I/O Init. OFh Initialize the local bus IDE IDE IDE Init. 10h Initialize Power Management 11h Load alternate registers with initial POST values 12h Restore CPU control word during warm boot 13h Initialize PCI Bus Mastering devices PCI Mast. Init. 14h Initialize PCI Bus Mastering devices PCI Mast. Init. 14h Initialize keyboard controller 16h BIOS ROM checksum BIOS Check sum 17h Initialize cache before memory autosize 18h 8254 timer initialization 1Ah 8237 DMA controller initialization 1Ch Reset Programmable Interrupt Controller 20h Test DRAM refresh RAM Refresh Test 22h Test 8742 keyboard controller 24h Set ES segment register to 4 GB 26h Enable A20 line 28h Autosize DRAM Memory Manager	06h	Initialize system hardware		
OAh Initialize CPU registers CPU Regist. Init OBh Enable CPU cache OCh Initialize caches to initial POST values OEh Initialize I/O component I/O Init. OFh Initialize the local bus IDE IDE Init. 10h Initialize Power Management 11h Load alternate registers with initial POST values 12h Restore CPU control word during warm boot 13h Initialize PCI Bus Mastering devices PCI Mast. Init. 14h Initialize keyboard controller 16h BIOS ROM checksum BIOS Check sum 17h Initialize cache before memory autosize 18h 8254 timer initialization 1Ah 8237 DMA controller initialization 1Ch Reset Programmable Interrupt Controller 20h Test DRAM refresh 22h Test 8742 keyboard controller 24h Set ES segment register to 4 GB 26h Enable A20 line 28h Autosize DRAM Memory Manager	08h	Initialize chipset with initial POST values		
OBh Enable CPU cache OCh Initialize caches to initial POST values OEh Initialize I/O component OFH Initialize the local bus IDE IDE Init. OFH Initialize the local bus IDE IDE Init. IOH Initialize Power Management Load alternate registers with initial POST values 12h Restore CPU control word during warm boot I3h Initialize PCI Bus Mastering devices PCI Mast. Init. I4h Initialize keyboard controller BIOS ROM checksum BIOS Check sum I7h Initialize cache before memory autosize I8h 8254 timer initialization IAh 8237 DMA controller initialization ICH Reset Programmable Interrupt Controller ZOH Test DRAM refresh RAM Refresh Test Z2h Test 8742 keyboard controller Keyb. Ctrl. Test 24h Set ES segment register to 4 GB Enable A20 line Autosize DRAM Memory Detection 3 Initialize POST Memory Manager	09h	Set IN POST flag	P.O.S.T Start	
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OEh Initialize I/O component I/O Init. OFh Initialize the local bus IDE IDE IDE Init. 10h Initialize Power Management 11h Load alternate registers with initial POST values 12h Restore CPU control word during warm boot 13h Initialize PCI Bus Mastering devices PCI Mast. Init. 14h Initialize keyboard controller 16h BIOS ROM checksum BIOS Check sum 17h Initialize cache before memory autosize 18h 8254 timer initialization 1Ah 8237 DMA controller initialization 1Ch Reset Programmable Interrupt Controller 20h Test DRAM refresh RAM Refresh Test 22h Test 8742 keyboard controller 24h Set ES segment register to 4 GB 26h Enable A20 line 28h Autosize DRAM Memory Manager	OBh	Enable CPU cache		
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1Ah 8237 DMA controller initialization 1Ch Reset Programmable Interrupt Controller 20h Test DRAM refresh RAM Refresh Test 22h Test 8742 keyboard controller Keyb. Ctrl. Test 24h Set ES segment register to 4 GB 26h Enable A20 line 28h Autosize DRAM Memory Detection 3 29h Initialize POST Memory Manager	17h	Initialize cache before memory autosize		
1Ch Reset Programmable Interrupt Controller 20h Test DRAM refresh RAM Refresh Test 22h Test 8742 keyboard controller Keyb. Ctrl. Test 24h Set ES segment register to 4 GB 26h Enable A20 line 28h Autosize DRAM Memory Detection 3 29h Initialize POST Memory Manager	18h	8254 timer initialization		
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24h Set ES segment register to 4 GB 26h Enable A20 line 28h Autosize DRAM Memory Detection 3 29h Initialize POST Memory Manager	20h	Test DRAM refresh	RAM Refresh Test	
26h Enable A20 line 28h Autosize DRAM Memory Detection 3 29h Initialize POST Memory Manager	22h	Test 8742 keyboard controller	Keyb. Ctrl. Test	
28h Autosize DRAM Memory Detection 3 29h Initialize POST Memory Manager	24h	Set ES segment register to 4 GB		
29h Initialize POST Memory Manager	26h	Enable A20 line		
	28h	Autosize DRAM	Memory Detection	3
2Ab Clay E19 VD boos DAM	29h	Initialize POST Memory Manager		
ZAII CIEGI 217 KR DASE KAMI	2Ah	Clear 512 KB base RAM		

Checkpoint Code	POST Routine Description	MaxiLife LCD Display Message	Beep Codes
2Ch	RAM failure on address line ¹	RAM Add. Failure	
2Eh	RAM failure on data bits xxxx ¹ of low byte of memory bus	RAM Data Low	
2Fh	Enable cache before system BIOS shadow		
30h	RAM failure on data bits $xxxx^1$ of high byte of memory bus	RAM Data High	
32h	Test CPU bus-clock frequency		
33h	Initialize POST Dispatch Manager		
36h	Warm start shut down		
38h	Shadow system BIOS ROM	Shadow BIOS ROM	
3Ah	Autosize cache		
3Ch	Advanced configuration of chipset registers		
3Dh	Load alternate registers with CMOS values		
42h	Initialize interrupt vectors		
45h	POST device initialization		
46h	Check ROM copyright notice		
48h	Check video configuration against CMOS		
49h	Initialize PCI bus and devices	PCI Detection	5
4Ah	Initialize all video adapters in system	Video Detection	4
4Bh	Display QuietBoot screen (optional)		
4Ch	Shadow video BIOS ROM		
4Eh	Display BIOS copyright notice		
50h	Display CPU type and speed		
51h	Initialize EISA board		
52h	Test keyboard	Keyboard Test	
54h	Set key click if enabled		

Order in Which POST Tests Are Performed

Checkpoint Code	POST Routine Description	MaxiLife LCD Display Message	Beep Codes
56h	Enable keyboard		
58h	Test for unexpected interrupts	Unexpect. STOP	
59h	Initialize POST display service		
5Ah	Display prompt "Press F2 to enter SETUP"		
5Bh	Disable CPU cache		
5Ch	Test RAM between 512 and 640 KB	Base Memory Test	
60h	Test extended memory	Ext. Memory Data	
62h	Test extended memory address lines	Ext. Memory Add.	
64h	Jump to UserPatch1		
66h	Configure advanced cache registers		
67h	Initialize Multi Processor APIC		
68h	Enable external and CPU caches		
69h	Setup System Management Mode (SMM) area		
6Ah	Display external L2 cache size		
6Ch	Display shadow-area message		
6Eh	Display possible high address for UMB recovery		
70h	Display error messages		
72h	Check for configuration errors		
76h	Check for keyboard errors	Keyboard Test	
7Ch	Set up hardware interrupt vectors		
7Eh	Initialize coprocessor if present		
80h	Disable onboard Super I/O ports and IRQs		
81h	Late POST device initialization		
82h	Detect and install external RS 232 ports		
83h	Configure non-MCD IDE controllers		

Checkpoint Code	POST Routine Description	MaxiLife LCD Display Message	Beep Codes
84h	Detect and install external parallel ports		
85h	Initialize PC-compatible PnP ISA devices		
86h	Re-initialize onboard I/O ports		
87h	Configure System Board Configurable Devices (optional)		
88h	Initialize BIOS Data Area		
89h	Enable Non-Maskable Interrupts (NMIs)		
8Ah	Initialize Extended BIOS Data Area		
8Bh	Test and initialize PS/2	Mouse PS2 Test	
8Ch	Initialize floppy controller		
8Fh	Determine number of ATA drives (optional)		
90h	Initialize hard disk controllers	Disc Ctrl. Init.	
91h	Initialize local-bus hard disk controllers	Disc Bus Init.	
92h	Jump to UsersPatch2	Maxilife Test	
93h	Build MPTABLE for multi-processor boards		
95h	Install CD-ROM for boot	CDROM Ctr. Init.	
96h	Clear huge ES segment register		
97h	Fix up Multi Processor table		
98h	Search for option ROMs.	Opt. Rom Detect.	
99h	Check for SMART drive		
9Ah	Shadow option ROMs		
9Ch	Set up Power Management		
9Dh	Initialize security engine (optional)		
9Eh	Enable hardware interrupts		
9Fh	Determine number of ATA and SCSI drives	Check ATA / SCSI	
AOh	Set time of day		

Checkpoint Code	POST Routine Description	MaxiLife LCD Display Message	Beep Codes
A2h	Check key lock		
A4h	Initialize typematic rate		
A8h	Erase F2 prompt		
AAh	Scan for F2 key stroke		
ACh	Enter SETUP	BIOS SETUP	
AEh	Clear Boot flag		
BOh	Check for errors	Checking	
B2h	POST done - prepare to boot operating system		
В5Н	Terminate QuietBoot (optional)		
B6h	Check password (optional)	Check Password	
B7h	ACPI tables initialized	ACPI Init.	
B8h	Clear global descriptor table		
B9h	Prepare Boot	Prepare Boot	
BAh	Initialize DMI parameters	DMI Tables Init.	
BBh	Initialize PnP Option ROMs	PNP Opt. ROM Init	
BCh	Clear parity checkers		
BDh	Display MultiBoot menu		
BEh	Clear screen (optional)		
BFh	Check virus and backup reminders		
COh	Try to boot with INT 19		
C1h	Initialize POST Error Manager (PEM)		
C2h	Initialize error logging		
C3h	Initialize error display function		
C4h	Initialize system error handling		
C5h	PnPnd dual CMOS (optional)		

Checkpoint Code	POST Routine Description	MaxiLife LCD Display Message	Beep Codes
C6h	Initialize notebook docking (optional)		
C7h	Initialize notebook docking late		
C8h	Force check (optional)		
C9h	Extended checksum (optional)		
D2h	Unknown Interupt		
The	e following are for boot block in Flash ROM		
EOh	Initialize the chipset		
E1h	Initialize the bridge		
E2h	Initialize the CPU		
E3h	Initialize system timer		
E4h	Initialize system I/O		
E5h	Check force recovery boot		
E6h	Checksum BIOS ROM		
E7h	Go to BIOS		
E8h	Set Huge Segment		
E9h	Initialize Multi Processor		
EAh	Initialize OEM special code		
EBh	Initialize PIC and DMA		
ECh	Initialize Memory type		
EDh	Initialize Memory size		
EEh	Shadow Boot Block		
EFh	System memory test		
FOh	Initialize interrupt vectors		
F1h	Initialize Run Time Clock		

6 Tests and Error Messages

Order in Which POST Tests Are Performed

Checkpoint Code	POST Routine Description	MaxiLife LCD Display Message	Beep Codes
F2h	Initialize video		
F3h	Initialize System Management Mode		
F4h	Output one beep before boot		
F5h	Boot to Mini DOS		
F6h	Clear Huge Segment		
F7h	Boot to Full DOS		

^{1.} If the BIOS detects error 2C, 2E, or 30 (base 512K RAM error), it displays an additional word-bitmap (xxxx) indicating the address line or bits that failed. For example:

[&]quot;2C 0002" means line 1 (bit one set) has failed.

[&]quot;2E 1020" means data bits 12 and 5 (bits 12 and 5 set) have failed in the lower 16 bits. The BIOS also sends the bitmap to the port-80 LED display. It first displays the checkpoint code, followed by a delay, the high-order byte, another delay, and then the low-order byte of the error. It repeats this sequence continuously.

Error Message Summary

In the event of an error generated in POST (Power-On-Self-Test) during the boot process, the Error Setup Manager gives access to one or more detected errors. Each EMU error is displayed as a 4-digit code with an associated text message on the monitor screen or/and the MaxiLife LCD panel.

Further details can be accessed by pressing ENTER. A detailed description of the reason for the failure and how to solve the problem is displayed. The following examples give the different types of error categories.

Category #1:	If the error is only a warning (i.e. key stuck), the POST should prompt:		
WARNING ¹			
00100	Keyboard Error		

^{1.} After a time-out period of five seconds without any intervention, the system resumes to boot.

Category #2: If the error is serious, the POST should prompt:

The BIOS has detected a serious problem that prevents your PC from booting

Press < Enter > to view more information about error

6 Tests and Error Messages

Error Message Summary

Code #	Cause / Symptom	Short message (US)
0000h	Any POST error that is not listed below	System error
0010h	CMOS Checksum error (if no Serial EEProm)	Incorrect CMOS Checksum
0011h	Date and Time (CMOS backed up from SE2P)	Date and Time Lost
0012h	PC configuration lost (both SE2P and CMOS lost)	Incorrect PC Configuration
0020h	Any POST error regarding an AT option ROM	Option ROM Error
0040h	Serial number corrupted (bad checksum or null #)	Invalid PC Serial Number
0041	Product flag not initialized or bad	Invalid Internal product type
0060h	RPO initialization failure	Remote Power On Error
0070h	CPU Termination Card missing from Processor 2 socket in a mono-processor system	CPU Terminator Card Error
0100h	Keyboard stuck key	Keyboard Error
0101h	Keyboard self-test failure	Keyboard Error
0102h	Keyboard controller I/O access failure	Keyboard Error
0103h	Keyboard not connected	Keyboard Error
0300h	Floppy A: self-test failure	Flexible Disk Drive A Error
0301h	Floppy B: self-test failure	Flexible Disk Drive B Error
0310h	Floppy A: not detected (but configured in CMOS)	Flexible Disk Drive Error
0311h	Floppy B: not detected (but configured in CMOS)	Flexible Disk Drive Error
0306h	General failure on floppy controller	Flexible Disk Drive Error
0400h	CD-ROM test failure	CD-ROM Error
0401h	CD-ROM not detected (but configured in CMOS)	CD-ROM Error
0500h	General failure on HDD onboard primary ctrl	IDE Device Error
0501h	General failure on HDD onboard secondary ctrl	IDE Device Error
0510h	HDD # 0 self-test error	IDE Device # 0 Error
0520h	HDD # 0 not detected (but configured in CMOS)	IDE Device # 0 Error
0521h	HDD # 1 not detected (but configured in CMOS)	IDE Device # 1 Error

Code #	Cause / Symptom	Short message (US)
0522h	HDD # 2 not detected (but configured in CMOS)	IDE Device # 2 Error
0523h	HDD # 3 not detected (but configured in CMOS)	IDE Device # 3 Error
0530h	Found a drive on slave connector only (primary)	IDE Device Error
0531h	Found a drive on slave connector only (secondary)	IDE Device Error
0600h	Found less video memory than configured in CMOS	Video Memory Error
0700h	Found less DRAM memory than at previous boot	System Memory Error
0711h	Defective SIMM (module 1, bank 1)	System Memory Error
0800h	Found lower cache size than configured	System Cache Error
0801h	Cache self-test failure	System Cache Error
0A00h	Plug and Play video auto-setting failure (DDC hang)	DDC Video Error

The following table summarizes the most significant of the problems that can be reported.

Message	Explanation or Suggestions for Corrective Action
Operating system not found	Check whether the disk, HDD, FDD or CD-ROM disk drive is connected. If it is connected, check that it is detected by POST. Check that your boot device is enabled on the Setup Security menu. If the problem persists, check that the boot device contains the operating system.
Missing operating system	If you have configured HDD user parameters, check that they are correct. Otherwise, use HDD type "Auto" parameters.
Resource Allocation Conflict -PCI device 0079 on system board	Clear CMOS.
Video Plug and Play interrupted or failed. Re-enable in Setup and try again	You may have powered your computer Off/On too quickly and the computer turned off Video plug and play as a protection.
System CMOS checksum bad - run Setup	CMOS contents have changed between 2 power-on sessions. Run Setup for configuration.
No message, system "hangs"	Check that the main memory modules are correctly set in their sockets.

6 Tests and Error Messages

Error Message Summary

Message	Explanation or Suggestions for Corrective Action
Other	An error message may be displayed and the computer may "hang" for 20 seconds and then beep. The POST is probably checking for a mass storage device which it cannot find and the computer is in Time-out Mode. After Time-out, run Setup to check the configuration.



Connectors and Sockets

IDE Drive Connectors

IDE Connectors			
Pin	Signal	Pin	Signal
1	Reset#	2	Ground
3	HD7	4	HD8
5	HD6	6	HD9
7	HD5	8	HD10
9	HD4	10	HD11
11	HD3	12	HD12
13	HD2	14	HD13
15	HD1	16	HD14
17	HD0	18	HD15
19	Ground 7	20	orientation key
21	DMARQ	22	Ground 2
23	DIOW#	24	Ground 3
25	DIOR#	26	Ground 4
27	IORDY	28	CSEL
29	DMACK#	30	Ground 5
31	INTRQ	32	IOCS16#
33	DA1	34	PDIAG#
35	DAO	36	DA2
37	CS1FX#	38	CS3FX#
39	DASP#	40	Ground 6

Flexible Disk Drive Data Connector			
Pin	Signal	Pin	Signal
1	Ground	2	LDENSEL#
3	Ground	4	Microfloppy
5	Ground	6	EDENSEL
7	Ground	8	INDX#
9	Ground	10	MTEN1#
11	Ground	12	DRSELO#
13	Ground	14	DRSEL1#
15	Ground	16	DTENO#
17	Ground	18	DIR#
19	Ground	20	STP#
21	Ground	22	WRDATA#
23	Ground	24	WREN#
25	Ground	26	TRKO#
27	Ground	28	WRPRDT#
29	Ground	30	RDDATA#
31	Ground	32	HDSEL1#
33	Ground	34	DSKCHG#

Battery Pinouts

Battery Connections		
Pin Signal		
1	GROUND	
2 VBAT1		
3	VBAT2	

Battery Connections	
Pin Signal	
1	VBAT1
2	GROUND

Additional SCSI LED Connector

A	Additional SCSI LED Connector (4-pin)		
Pin	Signal		
1	Not used		
2	LED Out		
3	LED Out		
4	Not used		

Power Supply Connector (20-pin) and Aux Power Connector

	Power Supply Connector for System Board (20-pin)			
Pin	Signal	Pin	Signal	
11	3V3_MAINSENSE	1	3V3_2	
12	12V_NEG	2	3V3_3	
13	GROUND_1	3	GROUND2	
14	_PSON	4	5V_1	
15	GROUND3	5	GROUND4	
16	GROUND5	6	5V_2	
17	GROUND6	7	GROUND7	
18	5V_NEG	8	PW0K	
19	5V_3	9	5VSB	
20	5V_4	10	12V	

Aux. Power Connector	
Pin	Signal
1	GROUND1
2	GROUND2
3	GROUND3
4	3V3_1
5	3V3_2
6	5V

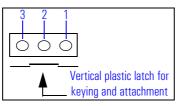
Wake On LAN Connector

Wake On LAN (WOL)		
Pin	Signal	
1	5V STDBY	
2	Ground	
3	LAN_WAKE	

Rear Fan Connector

Fan Connector	
Pin Signal	
1	Ground
2	12V Power
3	Sense

PCI Fan Connector (MT only)



	Fan Connector		
Pin	Signal		
1	Sense		
2	+ 12 V Power (or less, depending on desired fan speed)		
3	Ground		

Internal Audio Connectors

CD AUDIO Connector		
Pin Signal		1/0
1	Analog Ground	-
2	CD Left Channel	IN
3	Analog Ground	-
4	CD Right Channel	IN

	AUX Connector		
Pin	Signal	1/0	
1	Analog Ground	-	
2	AUX Left Channel	IN	
3	Analog Ground	-	
4	AUX Right Channel	IN	

Internal Speaker	
Pin	Signal
1	SPK1
2	Tst1
3	Tst2
4	SPK2

Status Panel and Intrusion

	Status Panel			
Pin	Pin Signal		Signal	
1	B1_LCD1	2	B1_LCD2	
3	Ground	4	PWR_LED_A	
5	HDD_LED_K	6	BACKLIGHT	
7	ON_OFF	8	RED-LED_A	
9	GROUND2	10	HDD_LED_A	
11	_RESET	12	SDA	
13	VSTDBY_3V	14	SCL	

Intrusion		
Pin Signal		
4	CLOSE	
3	COMMON	
1	OPEN	

Hard Disk Drive Temperature Connector

HDD Temperature		
Pin	Pin Signal	
1	3V3	
2	SENSE	
4	Ground	

VGA DB15 Connector

VGA DB Connector Pins			
Pin	Standard VGA	DDC2B	
1	Analog RED	Analog RED	
2	Analog GREEN	Analog GREEN	
3	Analog BLUE	Analog BLUE	
4	Monitor ID2	Monitor ID2	
5	n/c	DDC return	
6	Analog RED return	Analog RED	
7	Analog GREEN return	Analog GREEN	
8	Analog BLUE return	Analog BLUE	
9	n/c	V _{CC} supply (optional)	
10	Digital ground	Digital ground	
11	Monitor ID 0	Monitor ID 0	
12	Monitor ID 1	Data:SDA	
13	HSYNC	HSYNC	
14	VSYNC	VSYNC	
15	n/c	Clock:SCL	

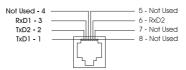
LCD Panel

LCD Panel				
Pin	Signal	Pin	Signal	
1	SCL_5V	2	VSTDBY 5V	
3	SDA_5V	4	BT_LCD 1	
5	not connected	6	BT_LCD 2	
7	RX_BB	8	TX_BB	
9	Ground	10	Ground	

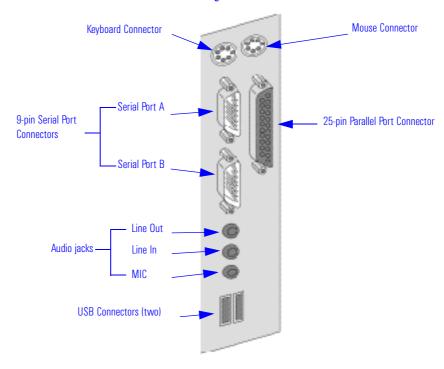
S-Video Connector



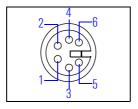
Ethernet UTP Connector



Rear Panel Socket Pin Layouts



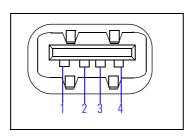
Keyboard and Mouse Connectors



	Keyboard and Mouse Connectors			
Pin	Signal	Pin	Signal	
1	Data	2	Not Used	
3	Ground	4	+ 5 V dc	
5	Clock	6	Not Used	

USB Stacked Connector

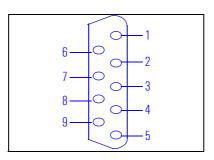
The USB graphic and pinout table for a USB connector. However, the information is also valid for a USB Stacked Connector.



USB Connector			
Pin	Signal		
1	VBus		
2	D-		
3	D+		
4	GND		
Shell	Shield		

Serial Port Connectors

This pinout information is valid for both the Serial Port A and Serial Port B connectors.

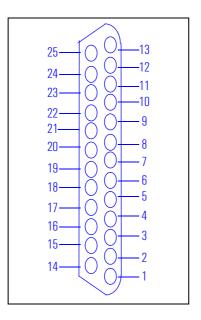


9-pin Serial Port Connector			
Pin	Signal	Pin	Signal
	1	1	(DCD) CF
6	(DSR) CC	2	(RD) BB
7	(RTS) CA	3	(TD) BA
8	(CTS) CB	4	(DTR) CD
9	(R) CE	5	(GND) AB

7 Connectors and Sockets

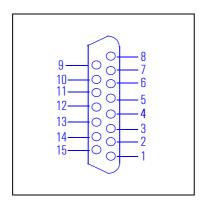
Rear Panel Socket Pin Layouts

25-pin Parallel Connector



25-pin Parallel Connector			
Pin	Signal	Pin	Signal
		13	SLCT
25	Ground	12	PE
24	Ground	11	BUSY
23	Ground	10	ACK
22	Ground	9	D7
21	Ground	8	D6
20	Ground	7	D5
19	Ground	6	D4
18	Ground	5	D3
17	SLIN	4	D2
16	INIT	3	D1
15	ERROR	2	D0
14	AUTO-FD	1	Strobe

MIDI/Joystick Connector



MIDI/Joystick Connector			
Pin	Signal	Pin	Signal
		8	+5 V
9	+5 V	7	A-2
10	B-1	6	A-Y
11	B-X	5	Ground
12	MIDI-OUT	4	Ground
13	B-Y	3	A-X
14	B-2	2	A-1
15	MIDI-IN	1	+5 V

External Audio Jacks

On the PC Workstation there is a Line In jack, Line Out jack and Mic In jack located on the rear panel. These external jacks are standard connectors.